FMA-HW01008-01 R01

| Rev. | Date | Author | Revision Description |
|---|---|---|---|
| R0A | 2018/05/08 | Kai Chuang | First release<br><br>2018/05/04<br>Change Part number from Samtec (119B00000199A) to All best ( 119B00000379A ). |
| | | | |
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 01_History | Kai Chuang |

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01_History
02_Index
03_Block Diagram
04_SMBUS
05_Clock
06_RESET
07_Power
08_Power Sequence
09_Strap Function
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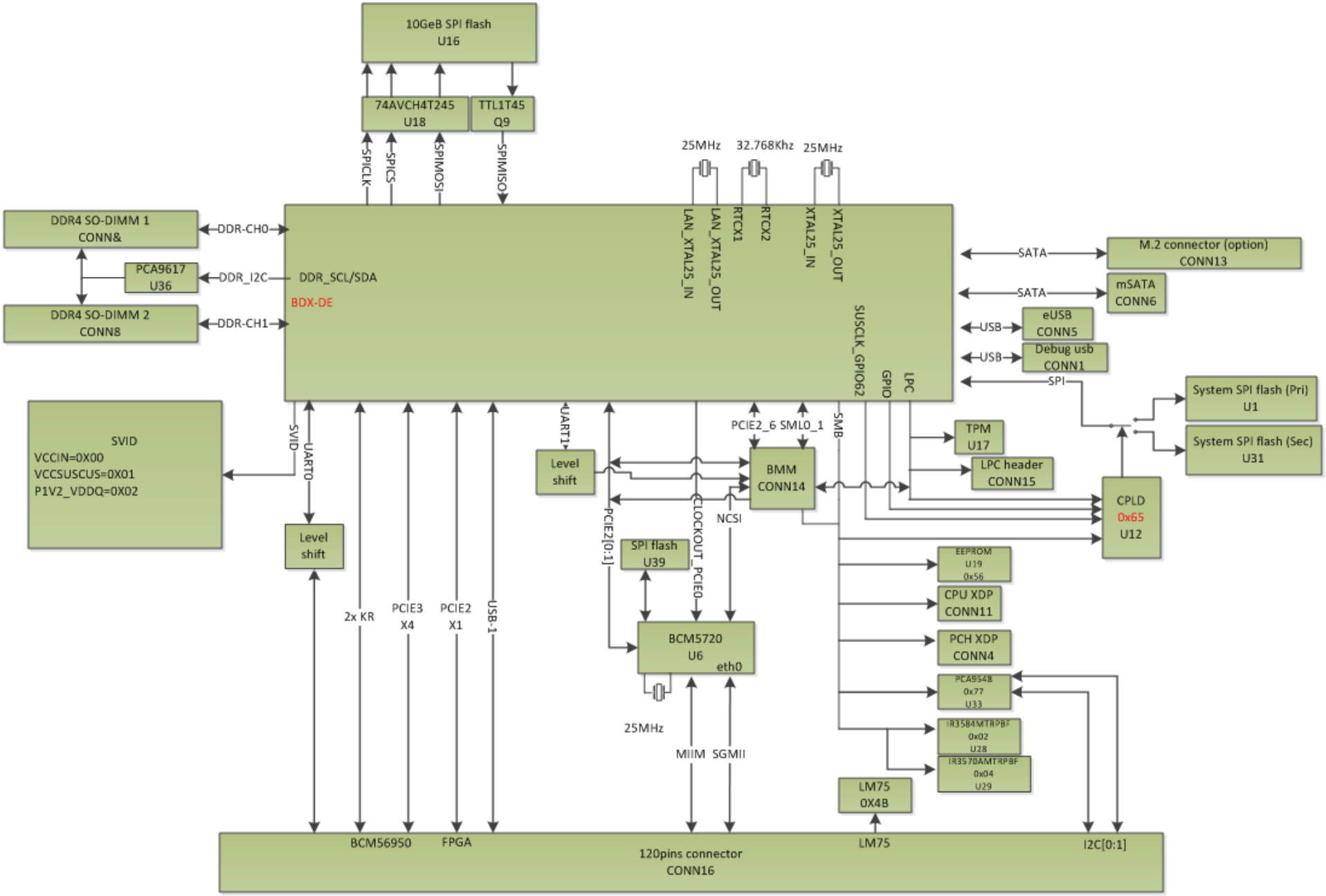
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| Size | Page Name | Engineer |
|---|---|---|
| C | 02_Index | Kai Chuang |

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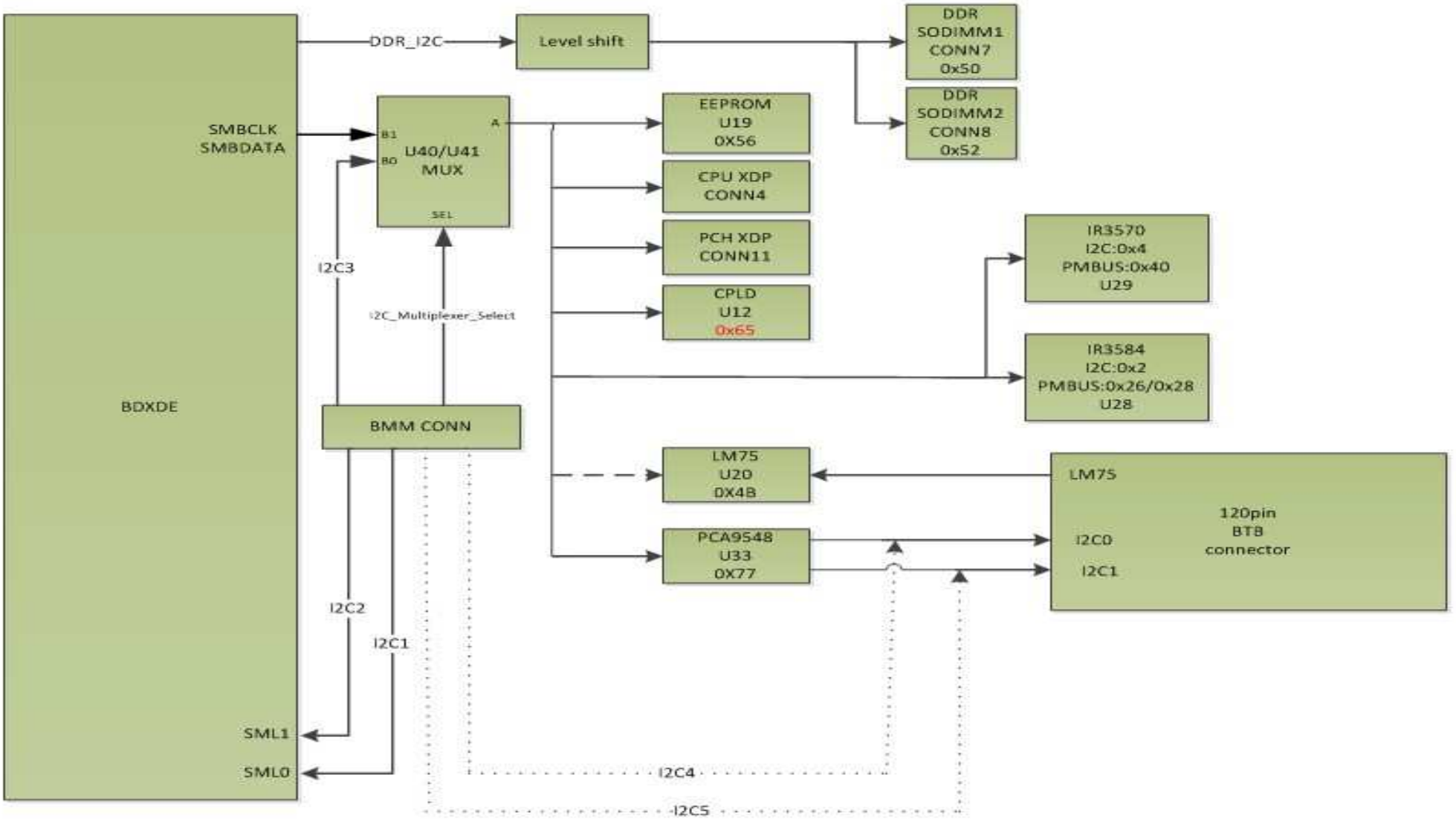

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| Size | Page Name | Engineer |
|---|---|---|
| C | 03_Block Diagram | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 3 of 39




Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

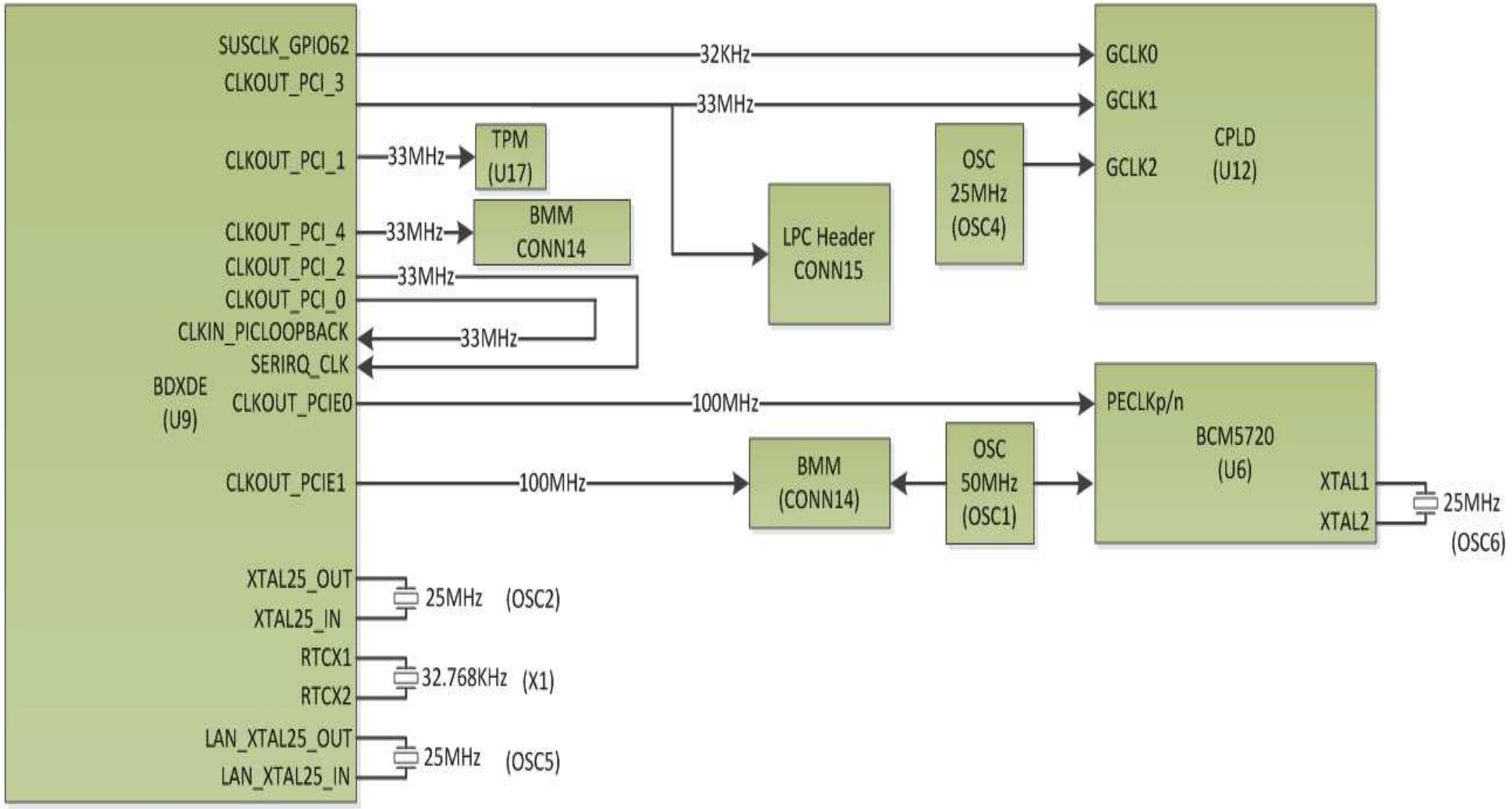
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| Size | Page Name | Engineer |
|---|---|---|
| C | 04_SMBUS | Kai Chuang |

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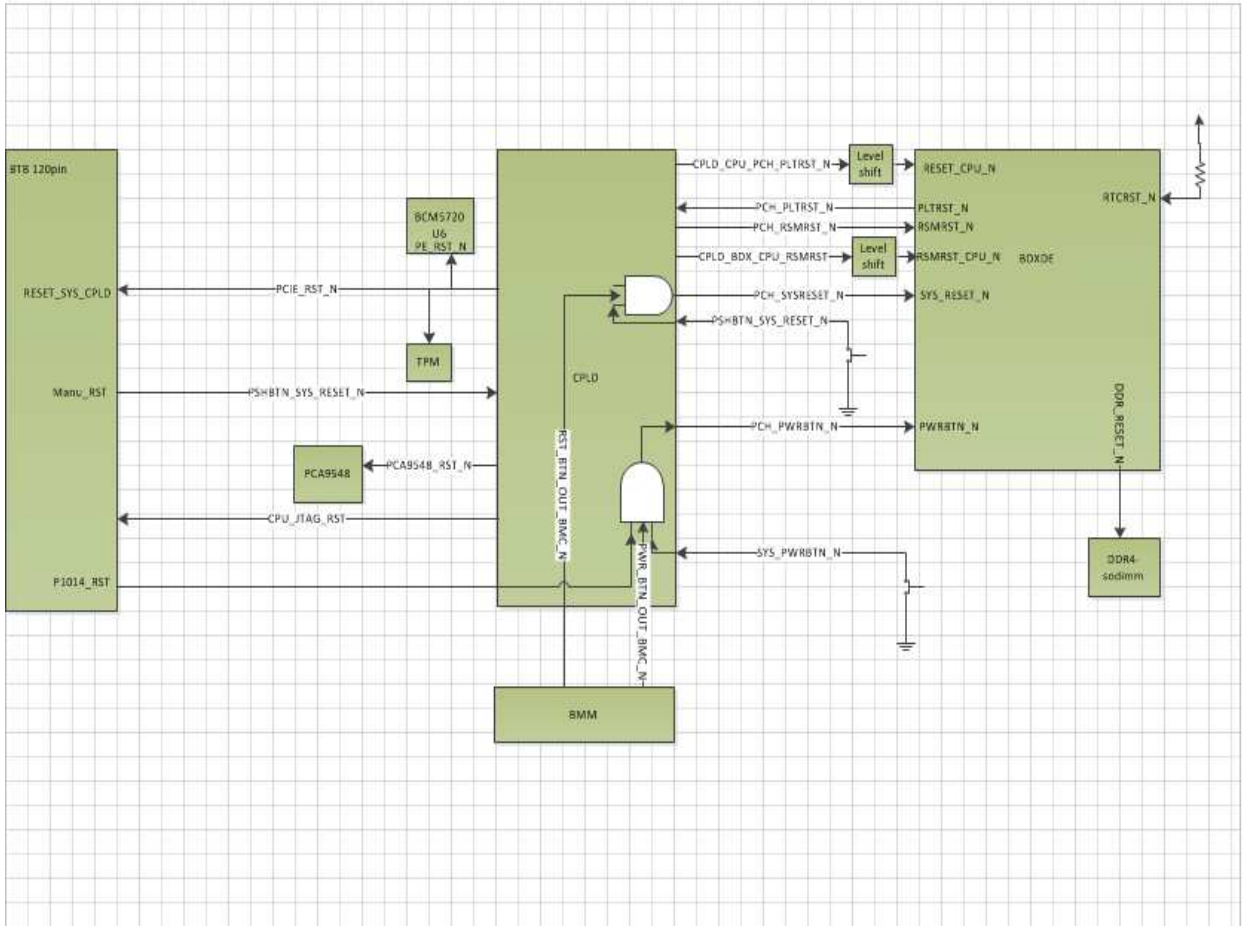

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| Size | Page Name | Engineer |
|---|---|---|
| C | 05_Clock | Kai Chuang |

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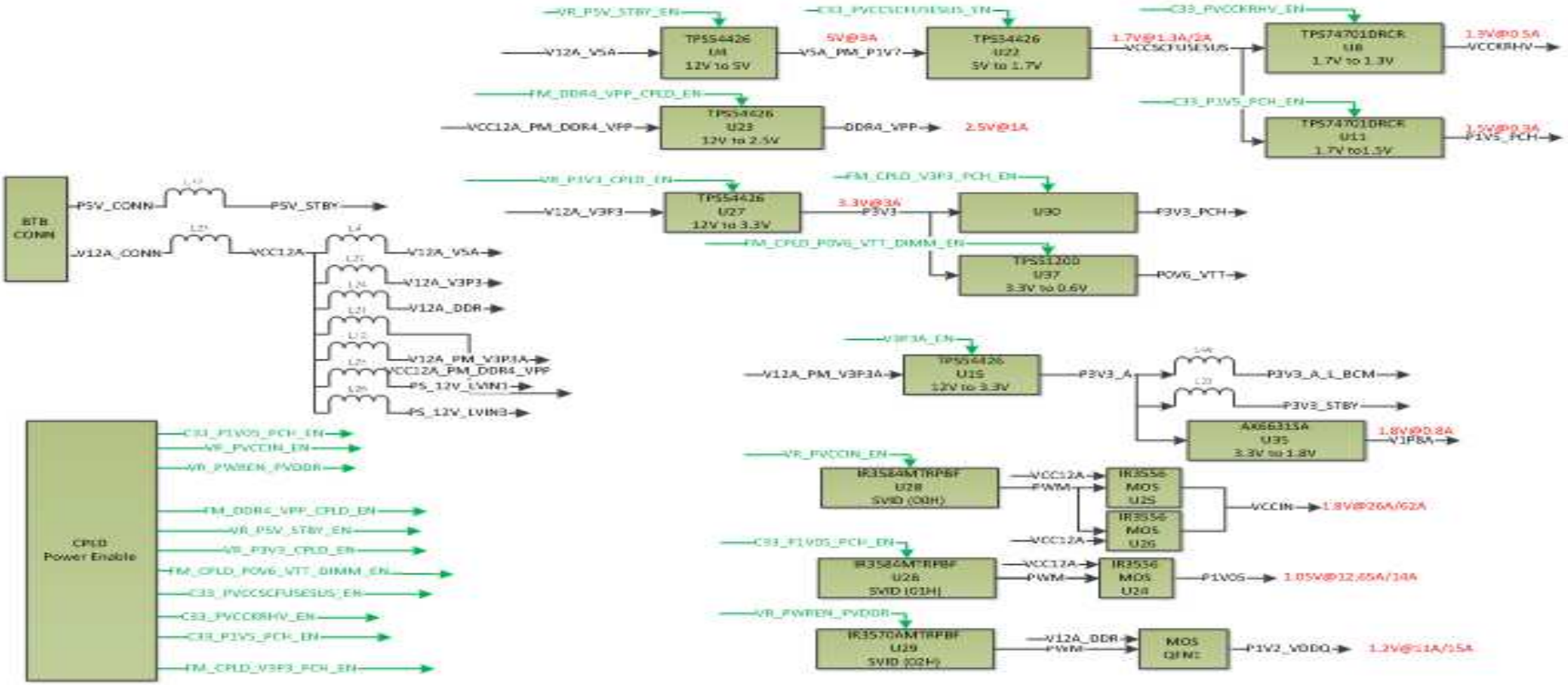

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| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 07_Power | Kai Chuang |

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## Grangeville / TBC

**CPLD**

- P3V3_A
- CPLD checks 12V good

**Standby rails**

- P5V_STBY
- P3V3_STBY
  - 10mS
  - Assert DPWROK
  - 1mS
  - Assert APWROK

**South Complex**

- VCCSCFUSESUS
- VCCIOIN
- VCCKRHV
- VCCGBE
- VCCSCSUS
  - 10mS
  - Assert SC_PWRGD
  - 10uS
  - Assert CPU_RSMRST

SLP_S4 transitions high

**Memory**

- DDR4_VPP
- P1V2_VDDQ
- P0V6_VTT_DIMM

**PCH Core**

- P1V05_PROC_IO
- P1V5_PCH
- P3V3

**CPU Core**

- VCCIN

Assert PCH_PWROK

1ms

Assert DRAM_PWROK

Assert SYS_PWRGD to PCH

PCH drives CPU_PWRGD_PCH to CPU

## Camelback Mountain

**CPLD**

- P3V3_A
- CPLD Checks 12V good

**Standby rails**

- P5V_STBY
- P3V3 (only standby rails come up)
  - 10mS
  - Assert DPWROK
  - 1mS
  - Assert APWROK

**South Complex**

- VCCSCFUSESUS
- P1V05
- VCCKRHV
- —Connected to P1V05
- —Connected to P1V05
  - 10mS
  - Assert SC_PWRGD
  - 10uS
  - Assert CPU_RSMRST

Camelback Mountain does not monitor SLP sig.

**Memory**

- DDR4_VPP
- P1V2_VDDQ
- P0V6_VTT_DIMM

**PCH Core**

- P1V05 comes up (ABOVE)
- P1V5_PCH
- P3V3_PCH – switched version of P3V3

**CPU Core**

- VCCIN

Assert PCH_PWROK

1mS

Assert DRAM_PWROK

Assert SYS_PWRGD to PCH

PCH Drives CPU_PWRGD_PCH

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|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 08_Power Sequence | Kai Chuang |

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## BroadWell_STRAP

| SIGNAL | VALUE | Note |
|---|---|---|
| LGSPARE4_DDR_STRAP | 0 | DDR3 |
| | 1 | DDR4 (Default) , IPU |
| PU_TXT_PLTEN | 0 | The platform is Intel TXT (Default) , IPU to 1.05 |
| | 1 | The platform is not Intel TXT |
| PU_TXT_AGENT | 0 | The socket is the Intel TXT Agent (default) , IPD |
| | 1 | The socket is not the Intel TXT Agent |
| ADR_STATUS_CLR | 0 | Disable Intel ME Crypto Transport Layer Security cipher suite (no confidentiality) internal PD , Default |
| | 1 | Enable Intel ME Crypto Transport Layer Security cipher suite (with confidentiality) |
| MANF_MODE_STRAP | 0 | Enable security measures defined in the Flash Descriptor (Default, IPD) |
| | 1 | Disable Flash Descriptor Security |
| BDX_INTVRMEN | 0 | DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source |
| | 1 | Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect. |
| CLK_M2_SUSCLK | 0 | Disable PLL On-Die voltage regulator |
| | 1 | Enable PLL On-Die voltage regulator (Default, IPU |
| PU_DSWODVREN | 0 | Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. |
| | 1 | Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards. (Default) |
| BDX_SPKR | 0 | Disable No Reboot mode. |
| | 1 | Enable No Reboot mode (default , IPD) |
| PU_GPIO51, XDP_NOA9_PCH) | 0 1 | RESERVED |
| | 1 0 | RESERVED |
| | 1 1 | BOOT from SPI (default) |
| | 0 0 | BOOT from LPC |
| GPIO33 | 0 | SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS (default , IPD) |
| | 1 | SoC TX is terminated to VCC/2. |
| BIST_ENABLE | 0 | Build-in Self Test Disable (Default) , IPU |
| | 1 | Build-in Self Test Enable |
| RP_UART1_TX | 0 | Disable NVM Security (Default) |
| | 1 | Security Enabled |
| ADR_STATUS_RD_R / GPIO36 | 0 | SoC RX is terminated to VSS (default , IPD) |
| | 1 | SoC RX is terminated to 1/2 VCC |
| PD_GPIO53 | 0 | SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. (Default) , IPU |
| | 1 | SoC is in DC-coupling mode. |
| FM_BIOS_RCRV_BOOT_N GPIO55 | 0 | Enable Top Swap mode. |
| | 1 | Disable Top Swap mode. , Default |
| BDX_CPLD_JTAG_ENABLE_R GPIO8 | | This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N. |
| MAC_INT_L_R / GPIO44 | | This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N. |
| CPU_JTAG_RST_R / GPIO46 | | This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N. |
| BMCINIT | 0 | Integrated Service Processor Boot Mode Disabled. (Default) , IPD |
| | 1 | Integrated Service Processor Boot Mode Enable |
| SAFE_MODE_BOOT | 0 | Safe Mode Boot Disabled (Default) , IPD |
| | 1 | Safe Mode Boot Enabled |
| DEBUG_EN_N XDP_CPU_PRESENT_N | 0 | Debug Mode |
| | 1 | Normal Mode |
| BDX_PECID0 | 0 | PECI_ID0 |
| LAN_NCSI_TRI_EN | 0 | PECI_ID1 |
| BDX_CPU2PCH_THROT | 0 | PECI_ID2 |
| RSVD12_AJ67 PD_BDX_SPARE4 | 0 | This pin should have a 5.1K ohm pull down to GND. There is weak internal pull down. |
| RSVD11_AG67 PD_BDX_SPARE3 | 0 | This pin should have a 5.1K ohm pull down to GND. There is weak internal pull down. |
| RSVD10_AN78 PD_BDX_SPARE2 | 0 | This pin should have a 5.1K ohm pull down to GND. There is weak internal pull down. |
| RSVD09_AC64 PD_BDX_SPARE1 | 0 | This pin should have a 5.1K ohm pull down to GND. There is weak internal pull down. |
| BDX_SERIRQ_DIR | 1 | Recommend 5.1k ohm pull up to VCCIOIN. There is no internal pull up or pull down. |
| UART_TXD[0] UART_BDX_TX0 | 0 | Recommend 5.1k ohm pull down to GND. There is no internal pull up or pull down. |
| UART_TXD[1] UART_BDX_TX1 | 0 | Disable NVM Security (Default) |
| | 1 | Security Enabled |
| PU_NCSI_RXD0 | 0 | Recommend 5.1K ohm pull up to VCCIOIN. There is no internal pull up or pull down. |
| PD_NCSI_RXD1 | 0 | LAN available in S5 for WoL |
| | 1 | LAN not available in S5. Manageability is disabled. (Default) |

## BroadWell_STRAP

| SIGNAL | VALUE | Note |
|---|---|---|
| (RP_LAN_MDIO_DIR_CTL_0, RP_LAN_MDIO_DIR_CTL_1) | 0,0 | Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1 |
| | 0,1 | Port 1 is disabled. Port 0 is enabled |
| | 1,0 | Reserved |
| | 1,1 | Both Port 0 and 1 are enabled. (Default) |
| RP_LAN_NCSI_ARB_OUT | 0 | Separate SVID controllers |
| | 1 | VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply (default) |

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|---|---|---|
| Model Name: BDX-DE CPU Board | | Rev: R0A |
| Size: C | Page Name: 09_Strap Function | Engineer: Kai Chuang |
| Date: Thursday, July 05, 2018 | Sheet 9 of 39 | |

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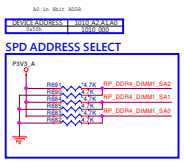
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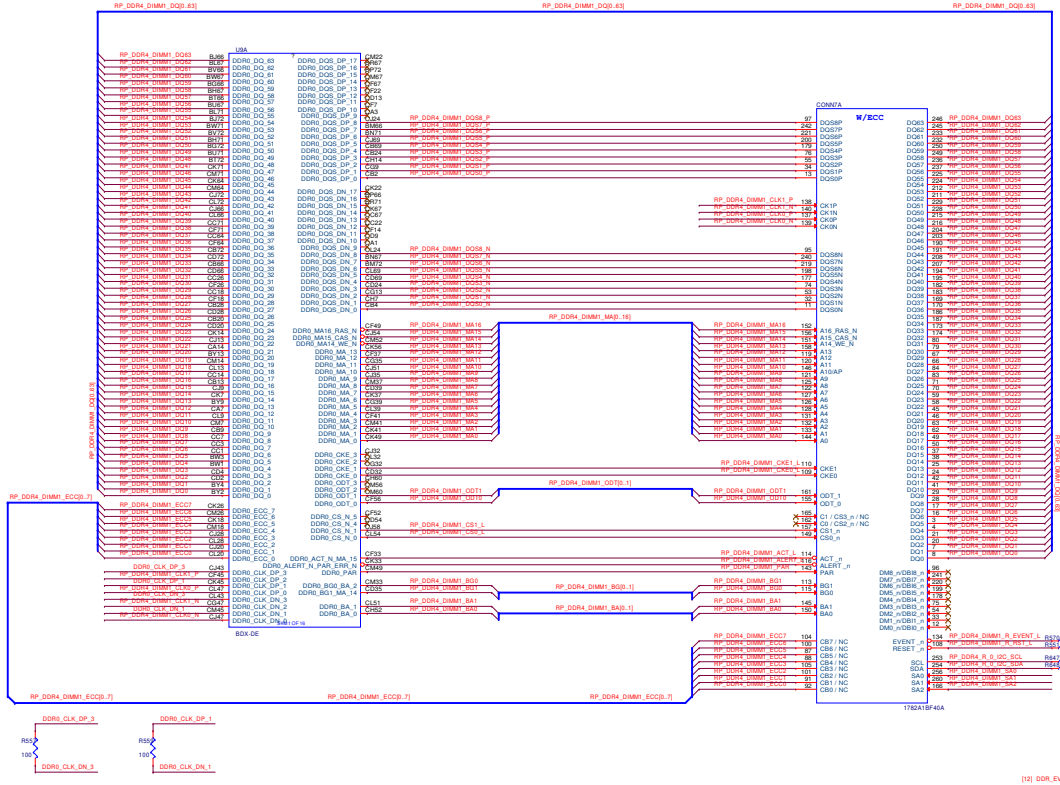
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|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 10_blank | Kai Chuang |

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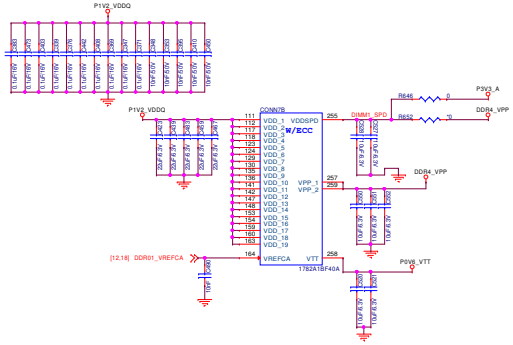



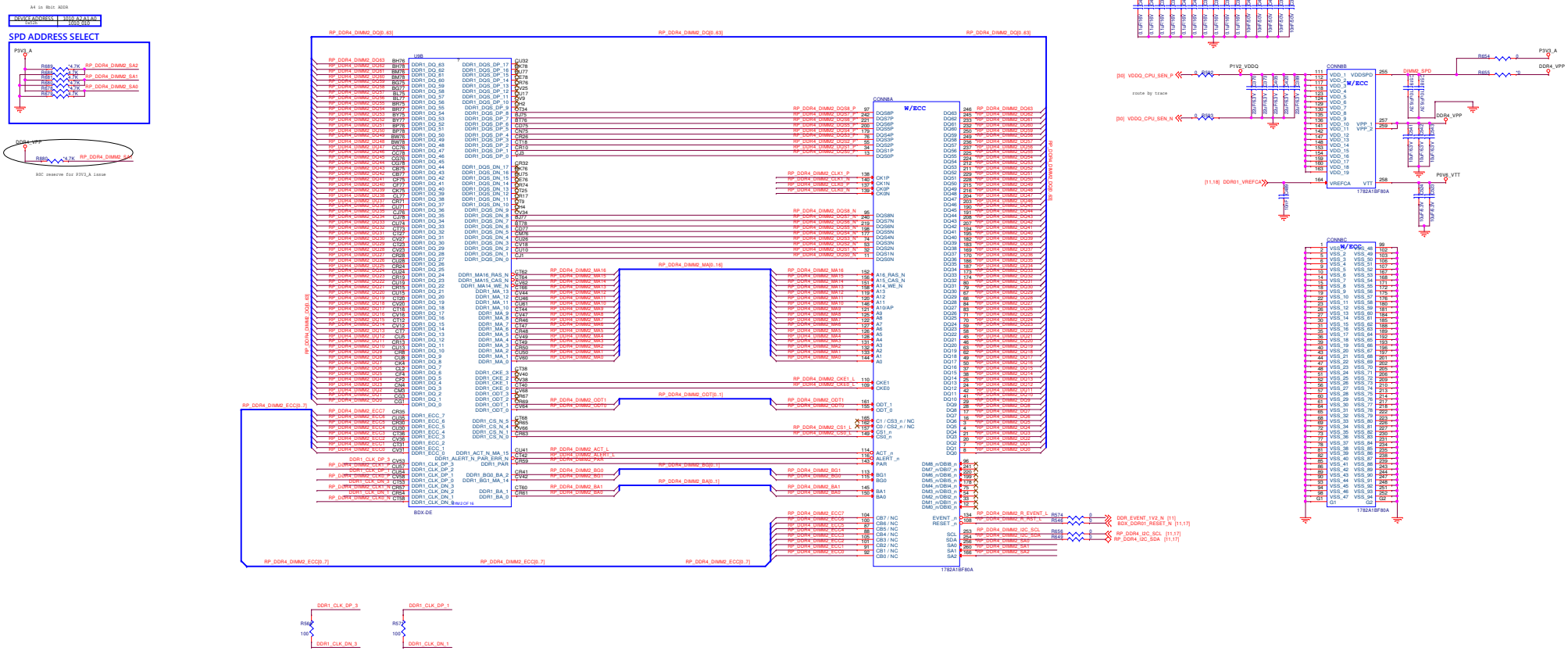

Table 4. Function table[5]

| Supply voltage | Input | Input/output[5] | |
|---|---|---|---|
| $V_{CCAN}$ $V_{CCBN}$ | DIR[3] | A | B |
| 0.8 V to 3.6 V | L | A = B | Input |
| 0.8 V to 3.6 V | H | Input | B = A |
| GND[6] | X | Z | Z |

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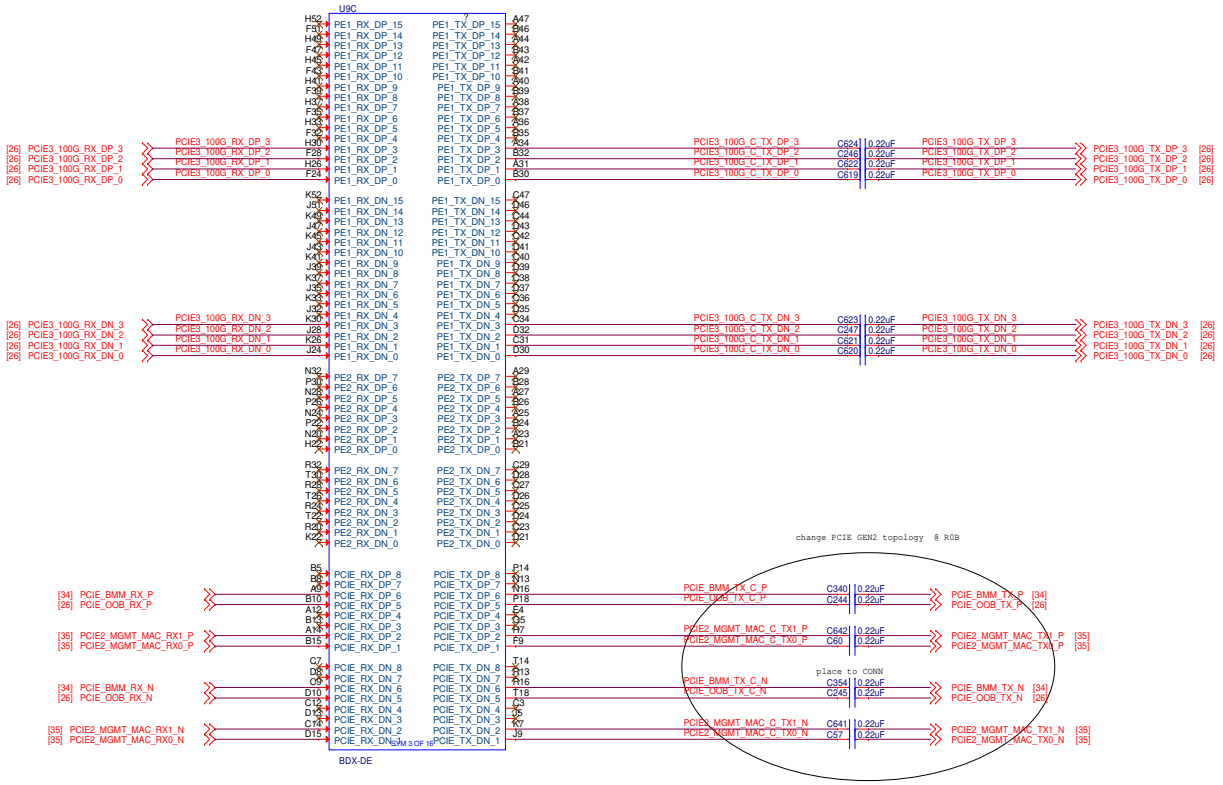
| | | | |
|---|---|---|---|
| Model Name | BDX-DE CPU Board | | Rev R0A |
| Size D | Page Name 11_RP_DDR4_SODIMM1 | Engineer Kai Chuang | |
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| Size D | Page Name 12_RP_DDR4_SODIMM2 | Engineer Kai Chuang | |
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| Size | Page Name | Engineer |
|---|---|---|
| C | 13_RP_PCIE | Kai Chuang |

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IXFT DFR SIGNALS

B2B to CPU

CPU to B2B

R0B Change, same as CRB

R0B change net name same as CRB

ASF5626 floating

Remove redundant CAPs

Change CL solution from PSE suggestion on R01

2 general purpose SDP Pins per port.
Can be used to support IEEE1588 auxiliary devices
or Input for external interrupts, etc.

R0B add

2018/06/06 Change U16 SPI flash from 107200000104A (EOL) W25Q32FVSSIG
WINBOND to 107200000211A
W25Q32JVSSIQ

**Table 1. FUNCTION TABLE(1) (each 2-bit section)**

| CONTROL INPUTS | | OUTPUT CIRCUITS | | OPERATION |
|---|---|---|---|---|
| OE | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A bus |
| L | H | Hi-Z | Enabled | A data to B bus |
| H | X | Hi-Z | Hi-Z | Isolation |

Table 4. Function table[1]

| Supply voltage | Input | Input/output[2] | |
|---|---|---|---|
| $V_{CCA}$, $V_{CCB}$ | DIR[3] | A | B |
| 0.8 V to 3.6 V | L | A = B | input |
| 0.8 V to 3.6 V | H | input | B = A |
| GND[3] | X | Z | Z |

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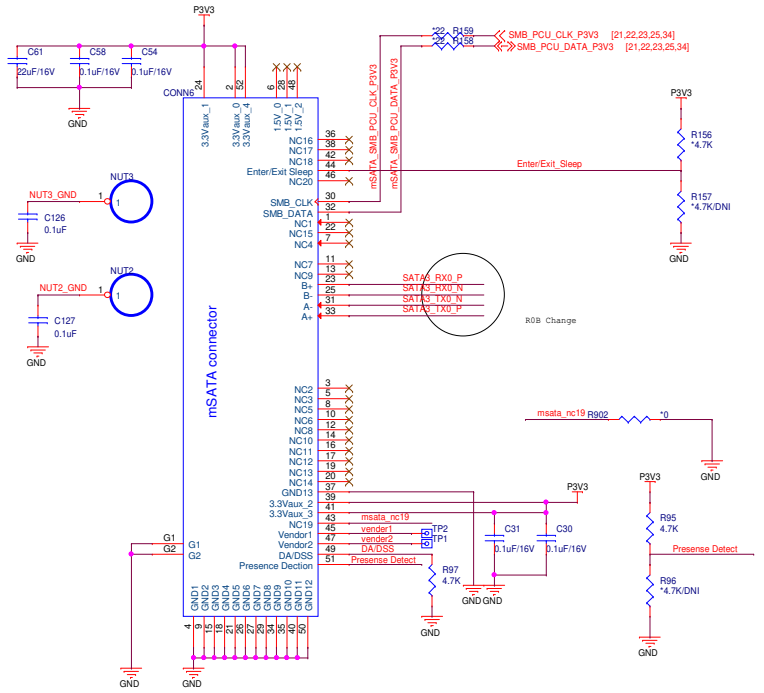
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| Model Name | Rev |
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| BDX-DE CPU Board | R0A |

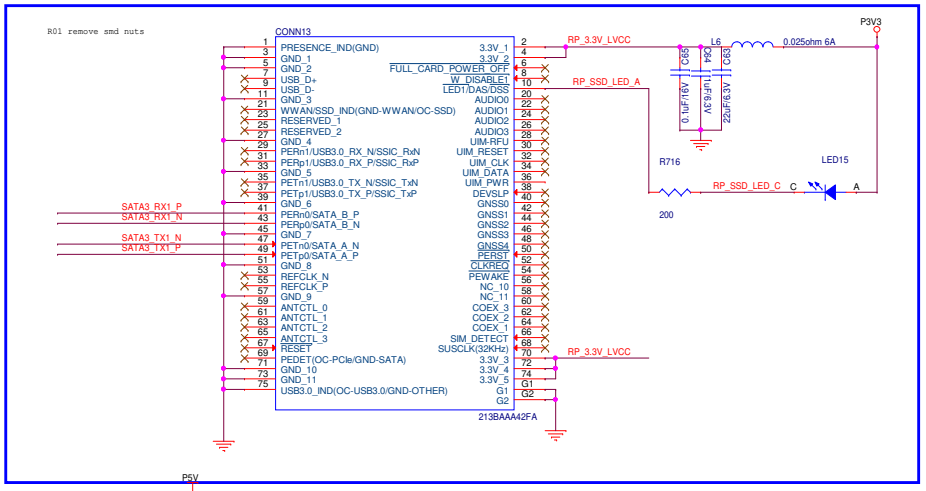
| Size | Page Name | Engineer |
|---|---|---|
| C | 14_BDX-DE_10GBEthernet | Kai Chuang |

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## mSATA CONN



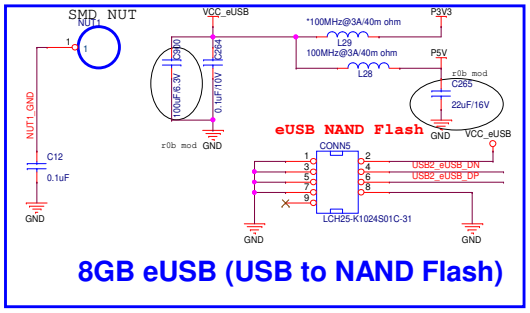

## M.2 CONN



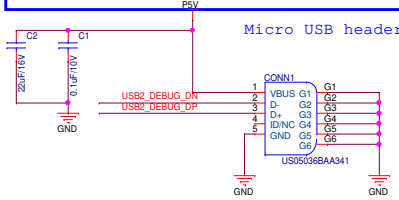

## mSATA CONNECTOR SIGNAL ASSIGNMENTS

| PIN# | NAME | PIN# | NAME |
|---|---|---|---|
| 51 | Presence Detection | 52 | +3.3V |
| 49 | DA/DSS | 50 | GND |
| 47 | Vendor | 48 | +1.5V |
| 45 | Vendor | 46 | Reserved |
| 43 | No Connect | 44 | Reserved |
| 41 | +3.3V | 42 | Reserved |
| 39 | +3.3V | 40 | GND |
| 37 | GND | 38 | Reserved |
| 35 | GND | 36 | Reserved |
| 33 | +A | 34 | GND |
| 31 | -A | 32 | Two Wire Interface |
| 29 | GND | 30 | Two Wire Interface |
| 27 | GND | 28 | +1.5V |
| 25 | -B | 26 | GND |
| 23 | +B | 24 | +3.3V |
| 21 | GND | 22 | Reserved |
| 19 | Reserved | 20 | Reserved |
| 17 | Reserved | 18 | GND |
| MECHANICAL KEY | | | |
| 15 | GND | 16 | Reserved |
| 13 | Reserved | 14 | Reserved |
| 11 | Reserved | 12 | Reserved |
| 9 | GND | 10 | Reserved |
| 7 | Reserved | 8 | Reserved |
| 5 | Reserved | 6 | +1.5V |
| 3 | Reserved | 4 | GND |
| 1 | Reserved | 2 | +3.3V |

## 8GB eUSB (USB to NAND Flash)




## Micro USB header




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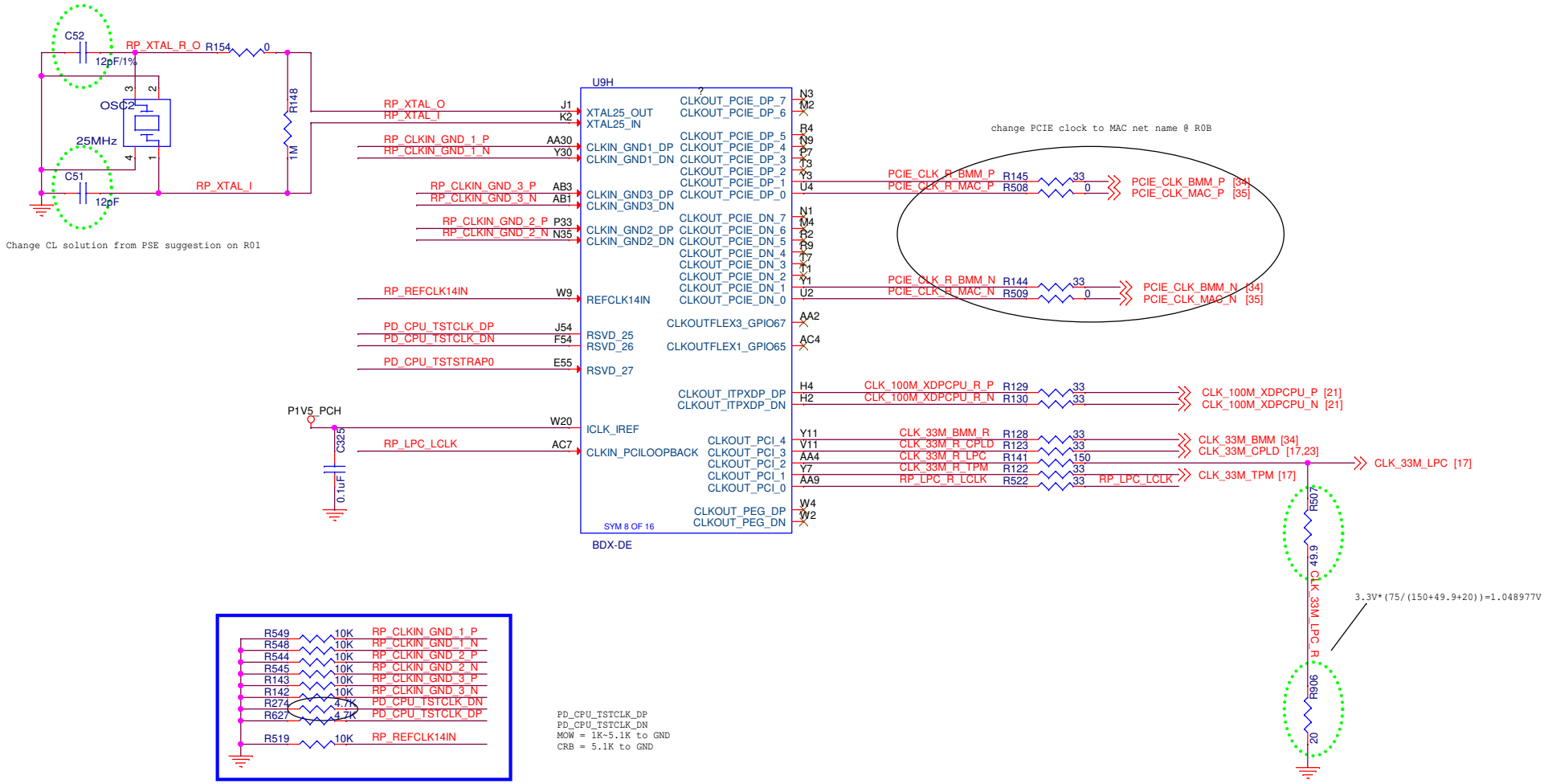
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| BDX-DE CPU Board | R0A |

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|---|---|---|
| C | 15_BDX-DE_SATA_USB | Kai Chuang |

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# FMA-HW01008-01 R01




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| Model Name: BDX-DE CPU Board | | Rev: R0A |
| Size: B | Page Name: 16_BDX-DE_Clock | Engineer: Kai Chuang |
| Date: Thursday, July 05, 2018 | Sheet 16 of 39 | |

# FMA-HW01008-01 R01

ST : R971, R972, R973 un-populated
Infineon : R971, R972, R973 populated

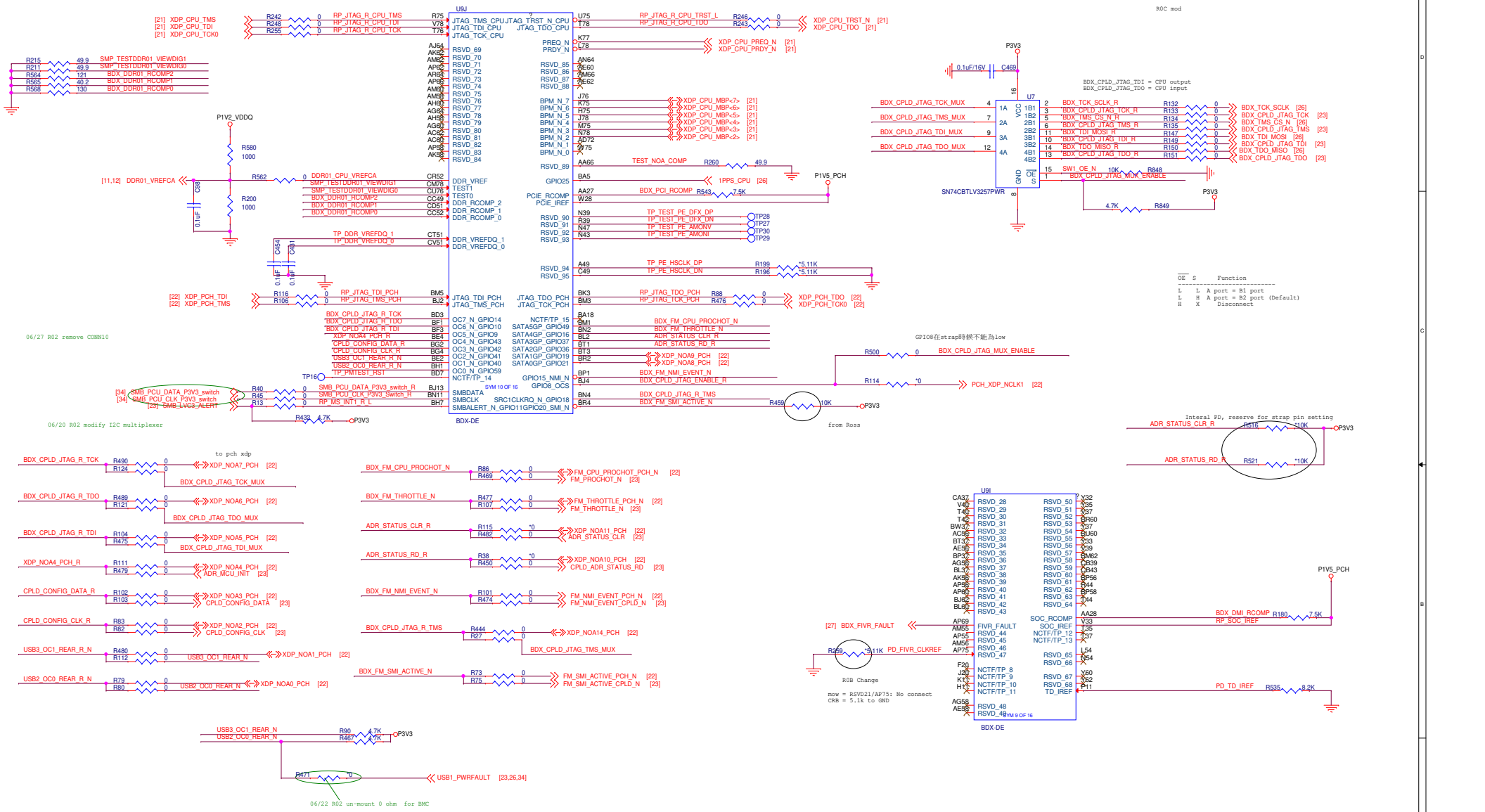
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| Size | Page Name | Engineer |
|---|---|---|
| D | 17_BDX-DE_SYSTEM | Kai Chuang |

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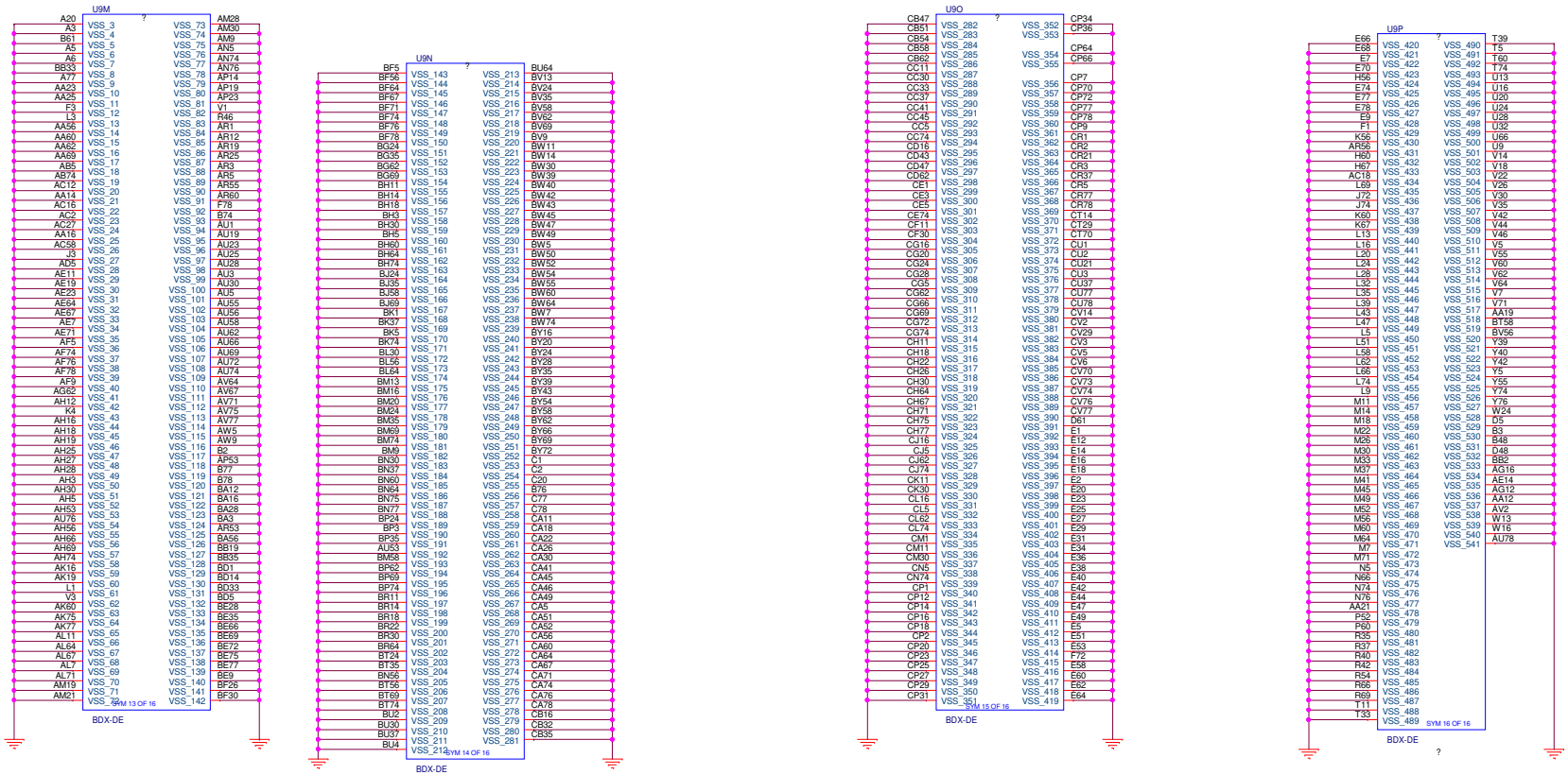

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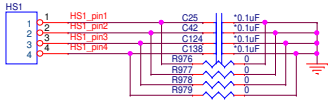
| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 18_BDX-DE_STRIP | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 18 of 39




2018/03/13 Update footprint.
Change footprint from hsink_60d_4dp_70wl17d3h to hsink_60d_4dp_70wl17d3h_os.
hsink_60d_4dp_70wl17d3h_osp要轉90度風流方向才會跟hsink_60d_4dp_70wl17d3h_1 一致
2018/04/13 Heatsink
Different of 117200000402A & 117200000618A is thermal pad.




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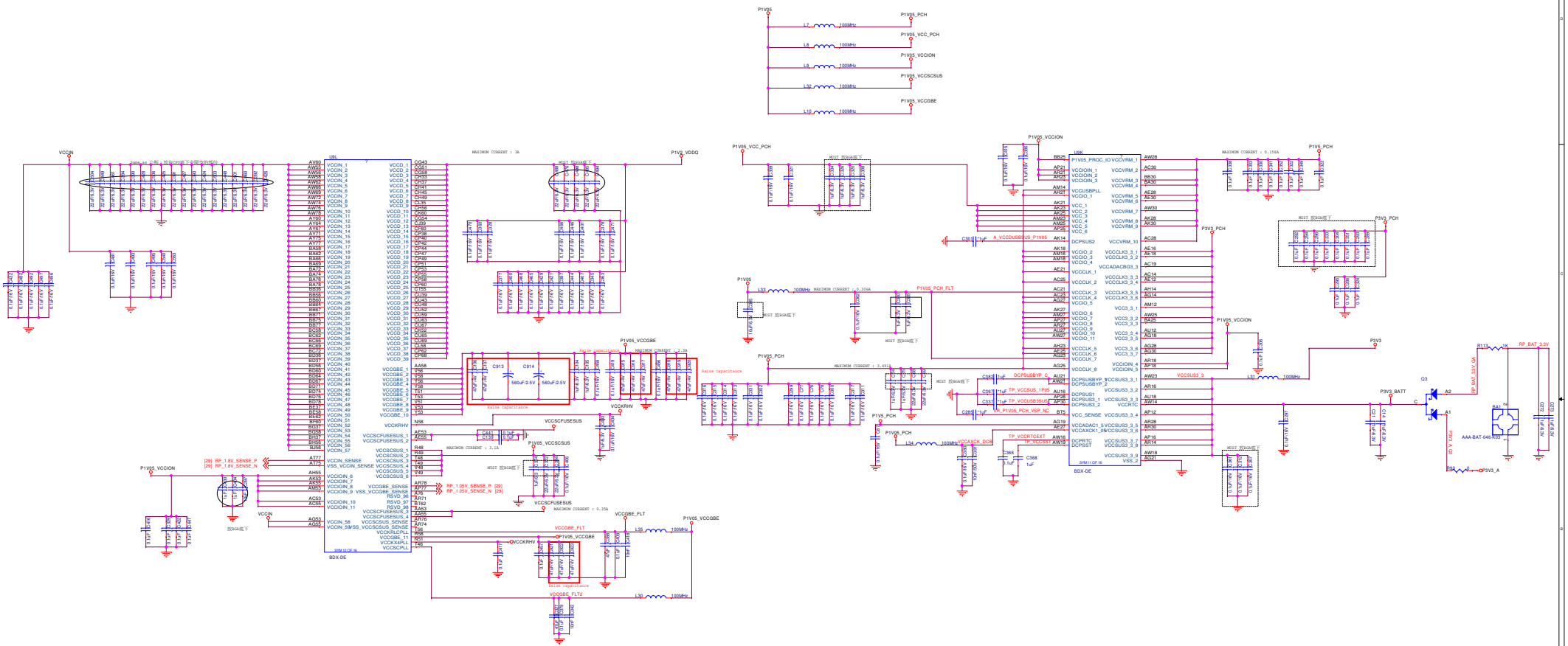
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 19_BDX-DE_GND | Kai Chuang |

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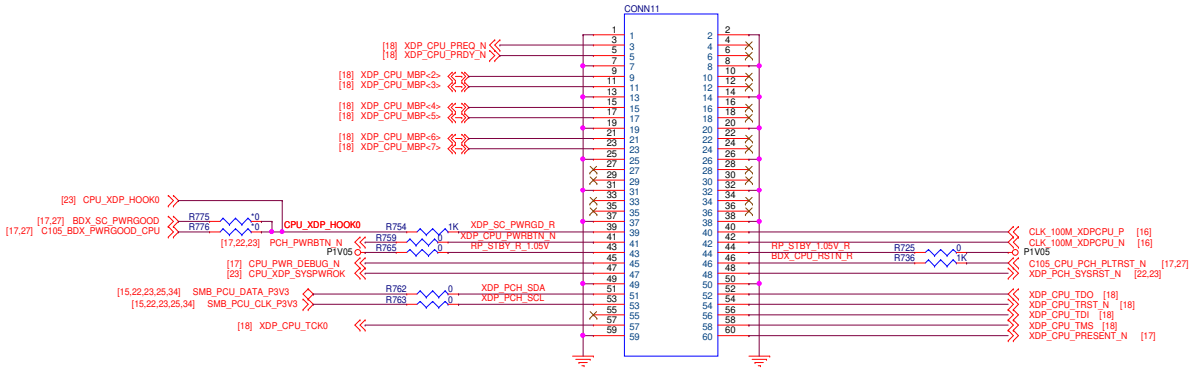
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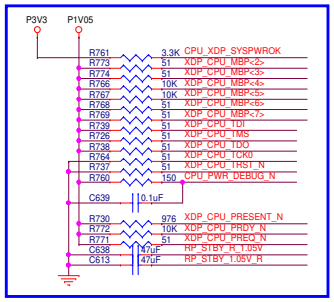
Accton
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| D | 20_BDX-DE_Power | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 20 of 39



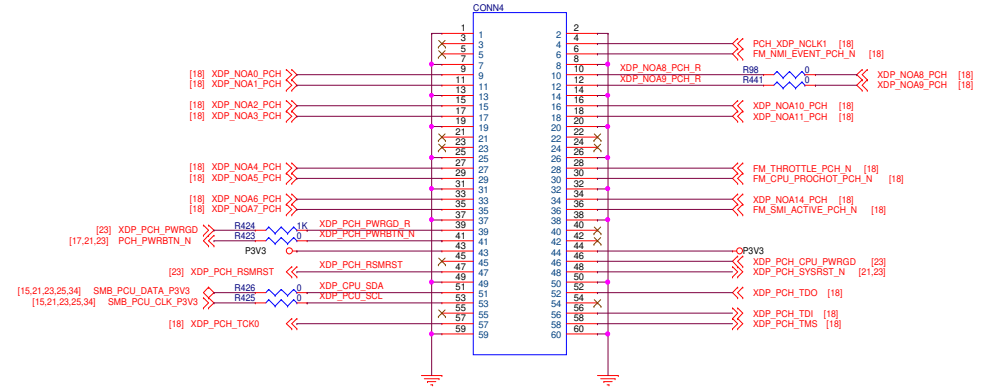

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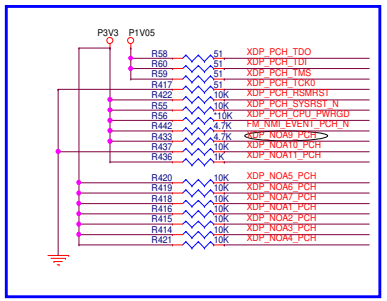
Accton
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C21 | _BDX-DE_CPU_XDP_CONN | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 21 of 39







GPIO51 / XDP_NOA9_PCH is the strap pin for BOOT setting

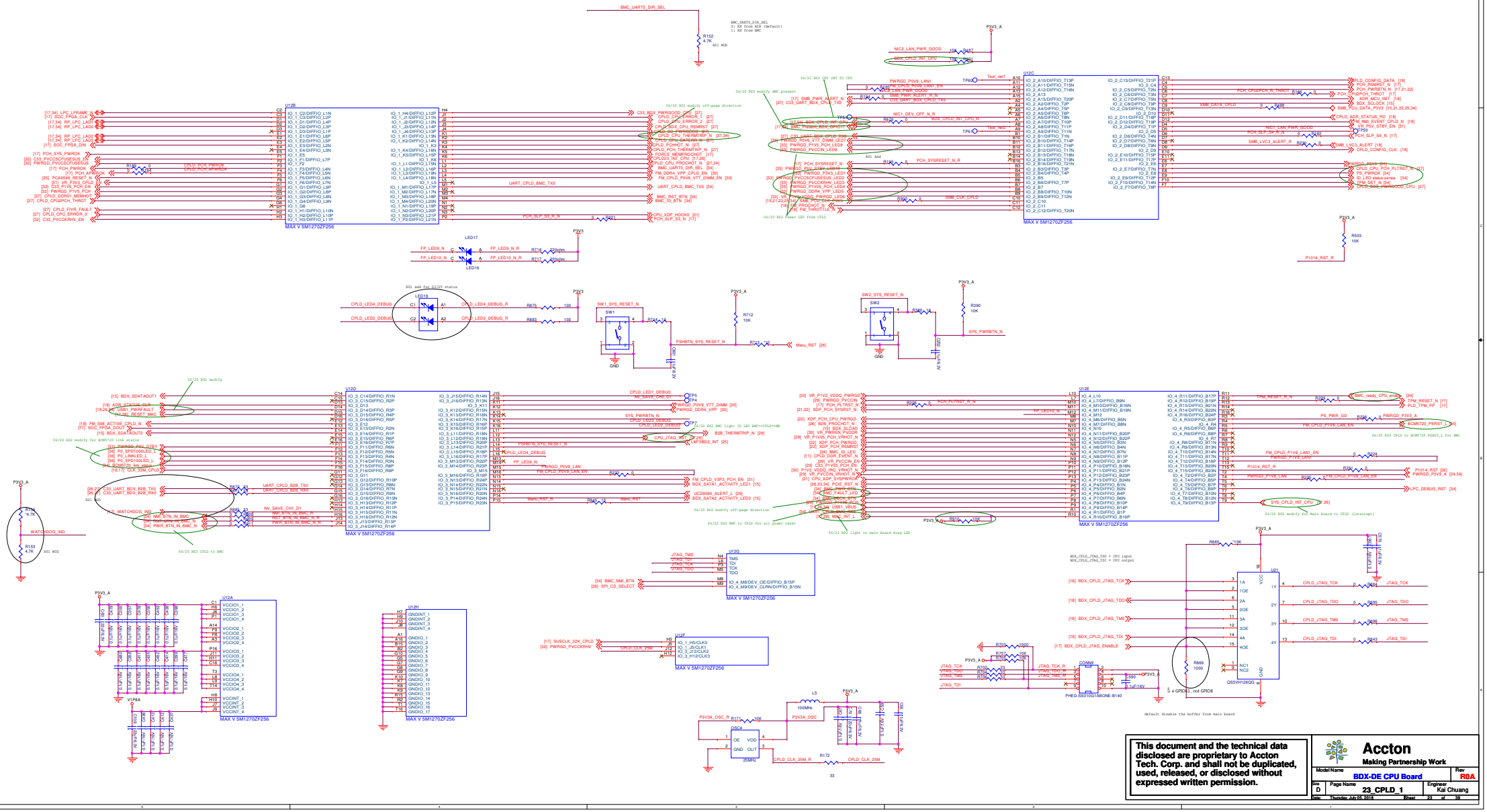
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 22_BDX-DE_PCH_XDP_CONN | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 22 of 39



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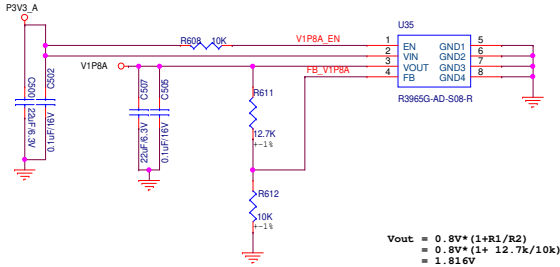
| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| D | 23_CPLD_1 | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 23 of 39

## 3.3V convert to 1.8V @0.8A For CPLD

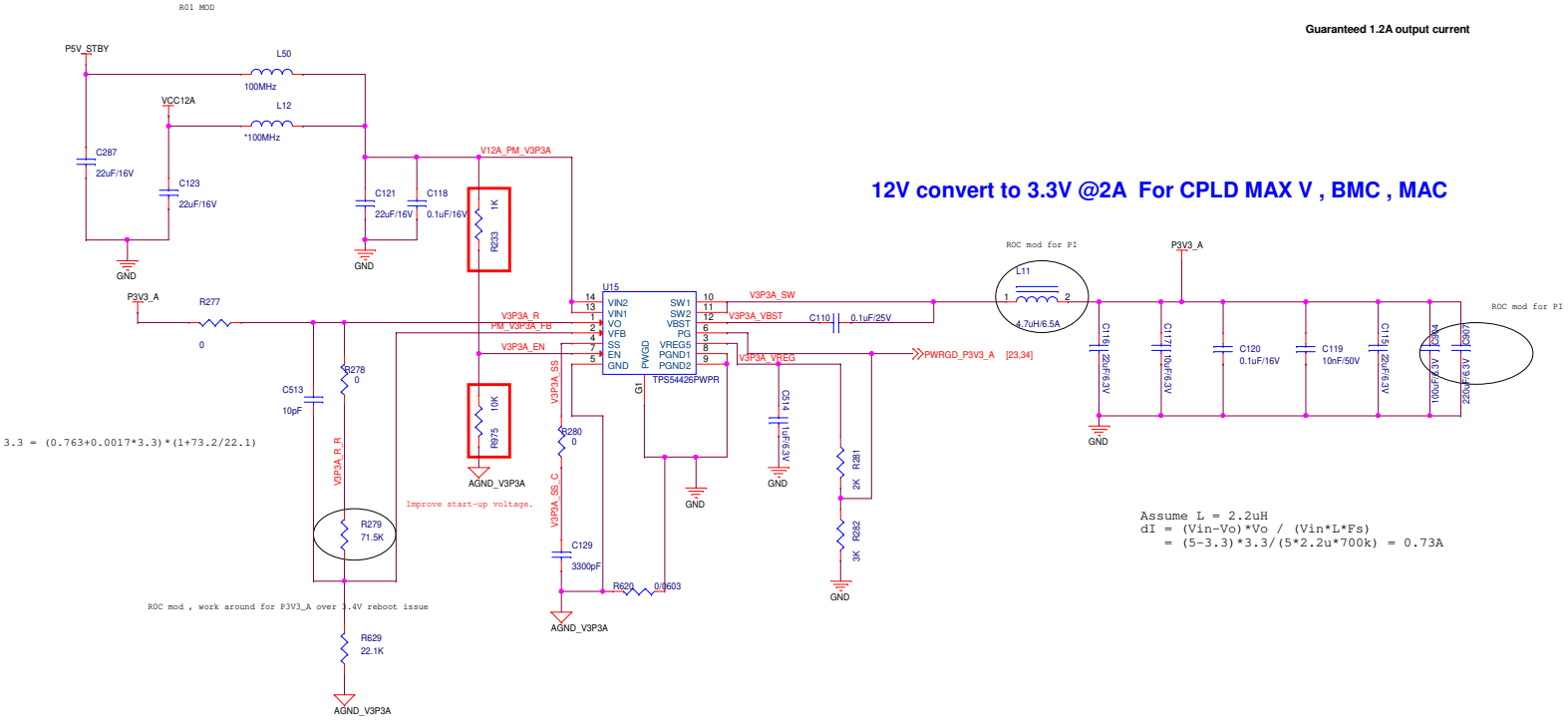
2018/02/06 Change U35
from 116800000089A to
116800000725AREG LDO
LR3965G-AD-S08-R ADJ
1.5A SO8 UTC




Vout = 0.8V*(1+R1/R2)
= 0.8V*(1+ 12.7k/10k)
= 1.816V

Guaranteed 1.2A output current

## 12V convert to 3.3V @2A For CPLD MAX V , BMC , MAC




Assume L = 2.2uH
dI = (Vin-Vo)*Vo / (Vin*L*Fs)
= (5-3.3)*3.3/(5*2.2u*700k) = 0.73A

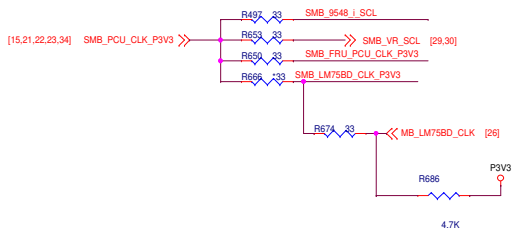
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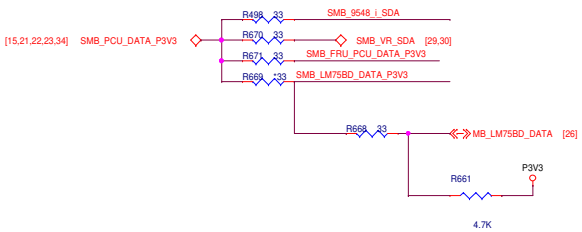
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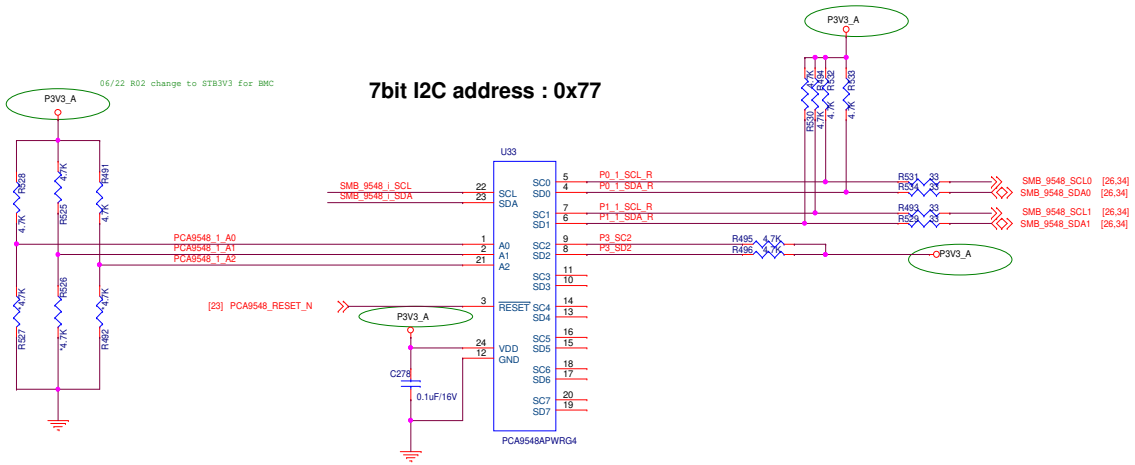
| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

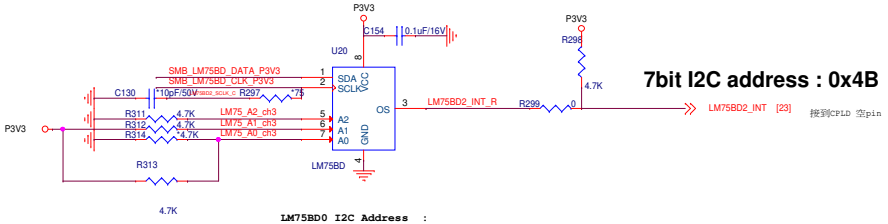
| Size | Page Name | Engineer |
|---|---|---|
| C | 24_CPLD_PWR_P3V3_A_P1V8A | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 24 of 39

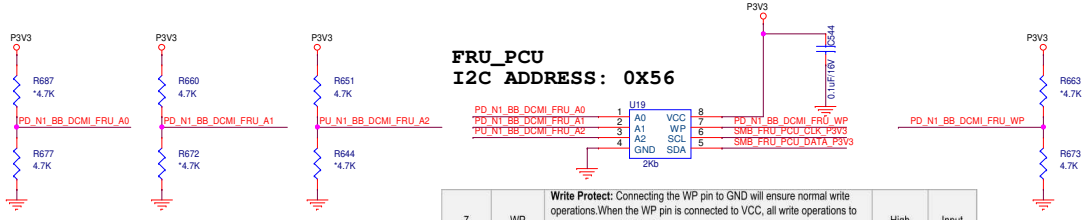



**LM75BD0 I2C Address :**
**1001 A2 A1 A0 :1001011**
**7Bit=>0X4B**



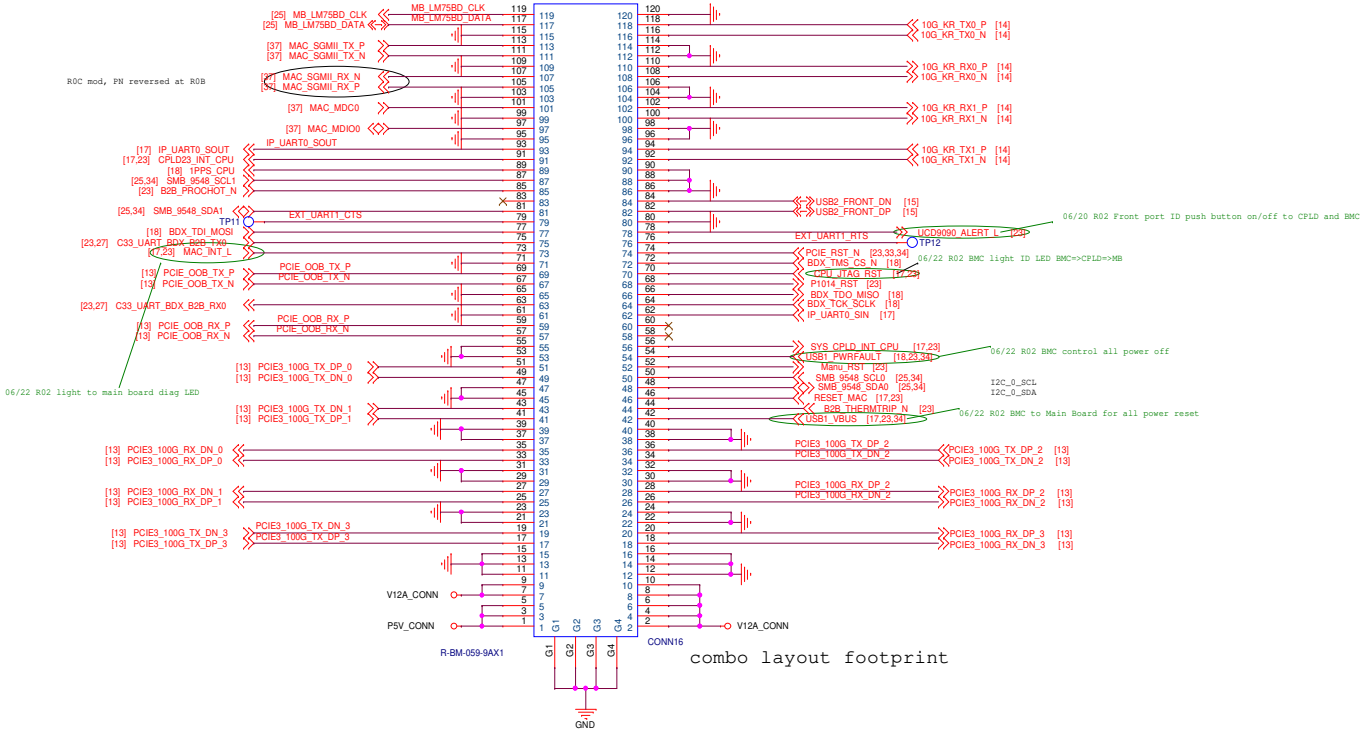

| | | | | |
|---|---|---|---|---|
| 7 | WP | **Write Protect:** Connecting the WP pin to GND will ensure normal write operations.When the WP pin is connected to VCC, all write operations to the memory are inhibited.<br>Refer to Note 1 for behavior of the pin when not connected. | High | Input |

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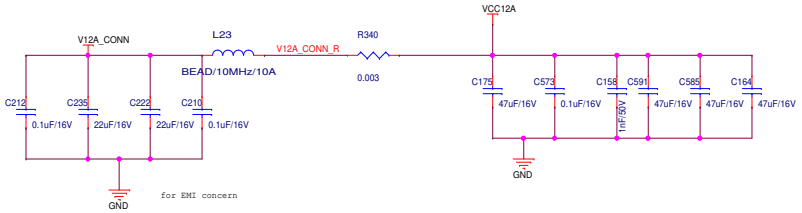
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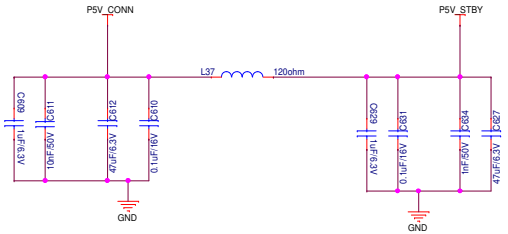
| | | |
|---|---|---|
| Model Name | BDX-DE CPU Board | Rev R0A |
| Size C | Page Name 25_SMBUS Device | Engineer Kai Chuang |
| Date: Thursday, July 05, 2018 | Sheet 25 of 39 | |

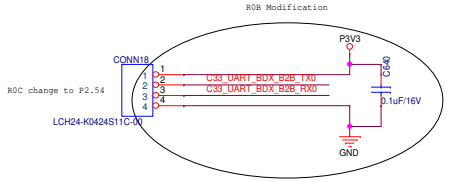
**footprint改成connm_d5x5d32_2x60sp_combo_1**
**2018/05/04**
**Change Part number from Samtec (119B00000199A) to All best ( 119B00000379A ).**




combo layout footprint



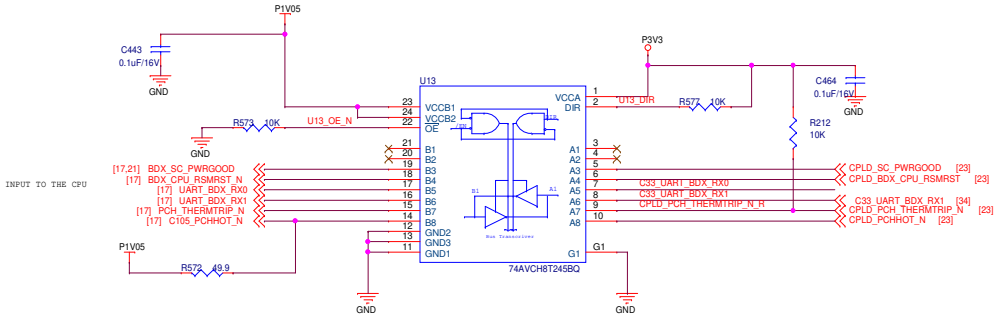

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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 26_B2B Connector | Kai Chuang |

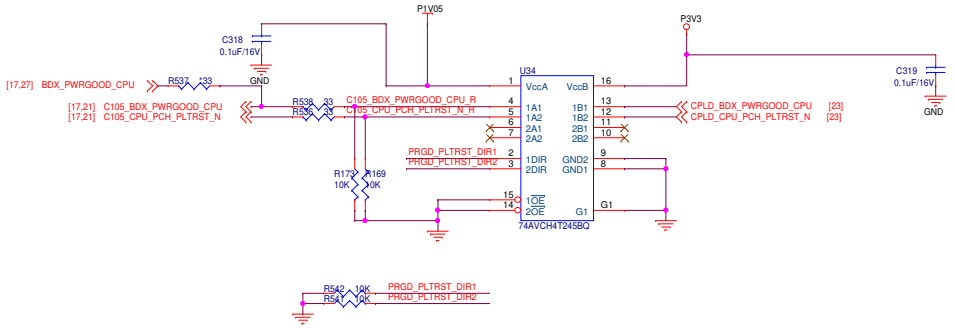
Date: Thursday, July 05, 2018 Sheet 26 of 39

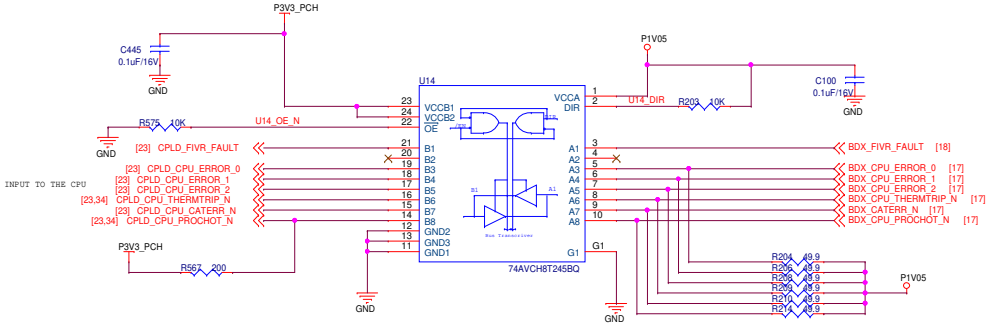


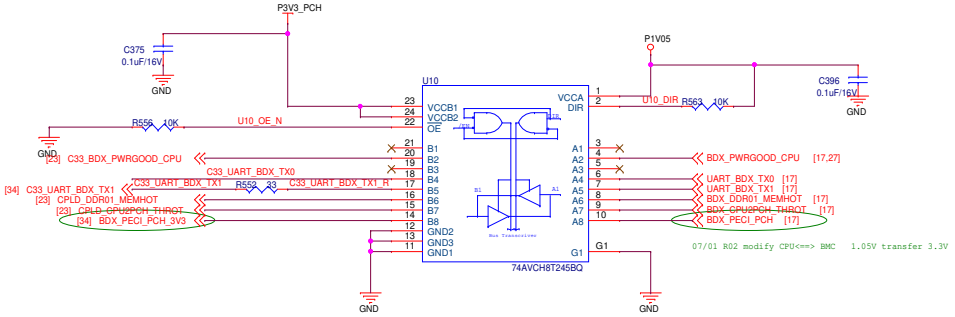

**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | All outputs Hi-Z |




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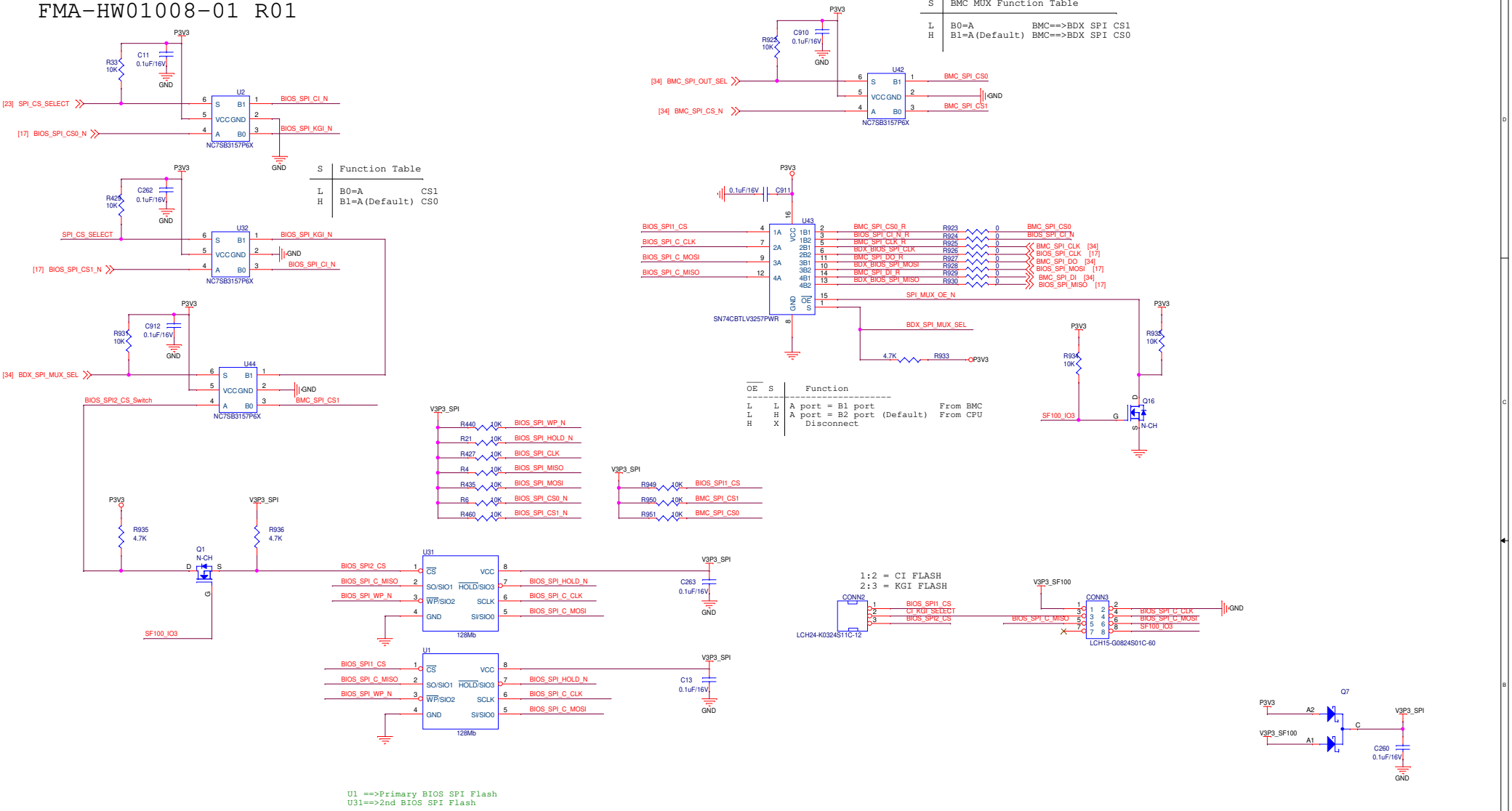
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 27_Level Shifter | Kai Chuang |

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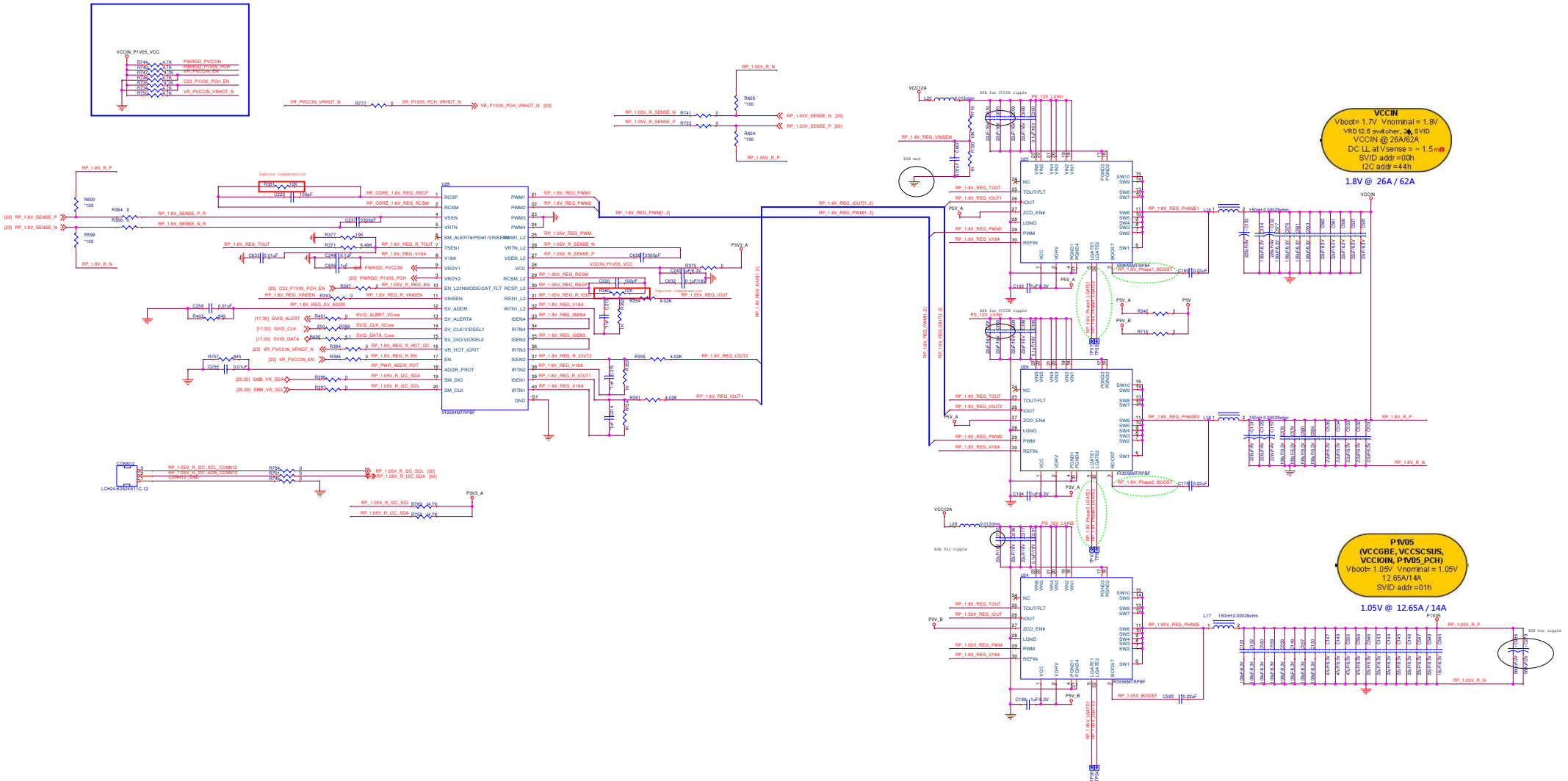
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| C | 28_SPI | Kai Chuang |

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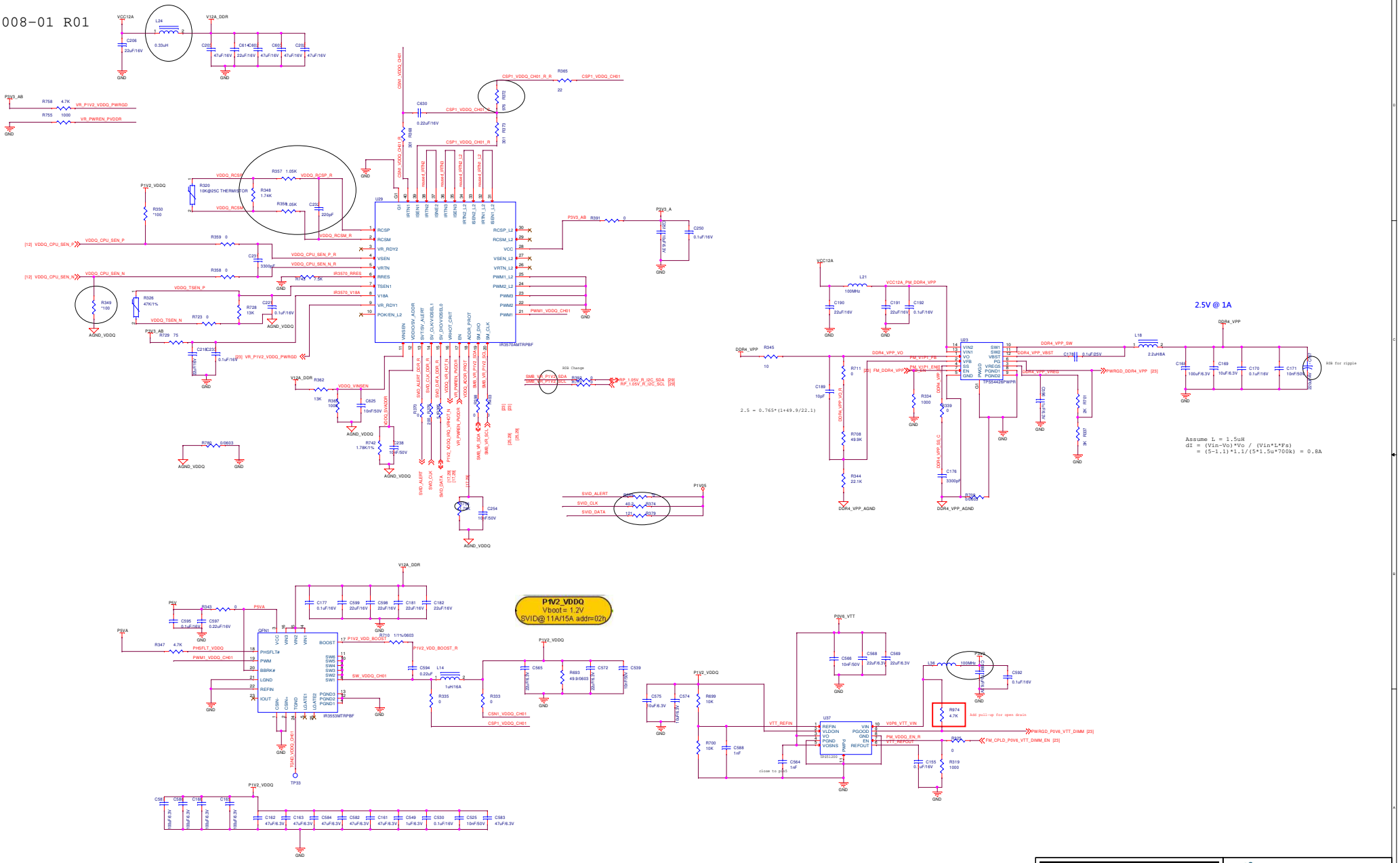
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| D | 29_VCCIN_P1V05 | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 29 of 39

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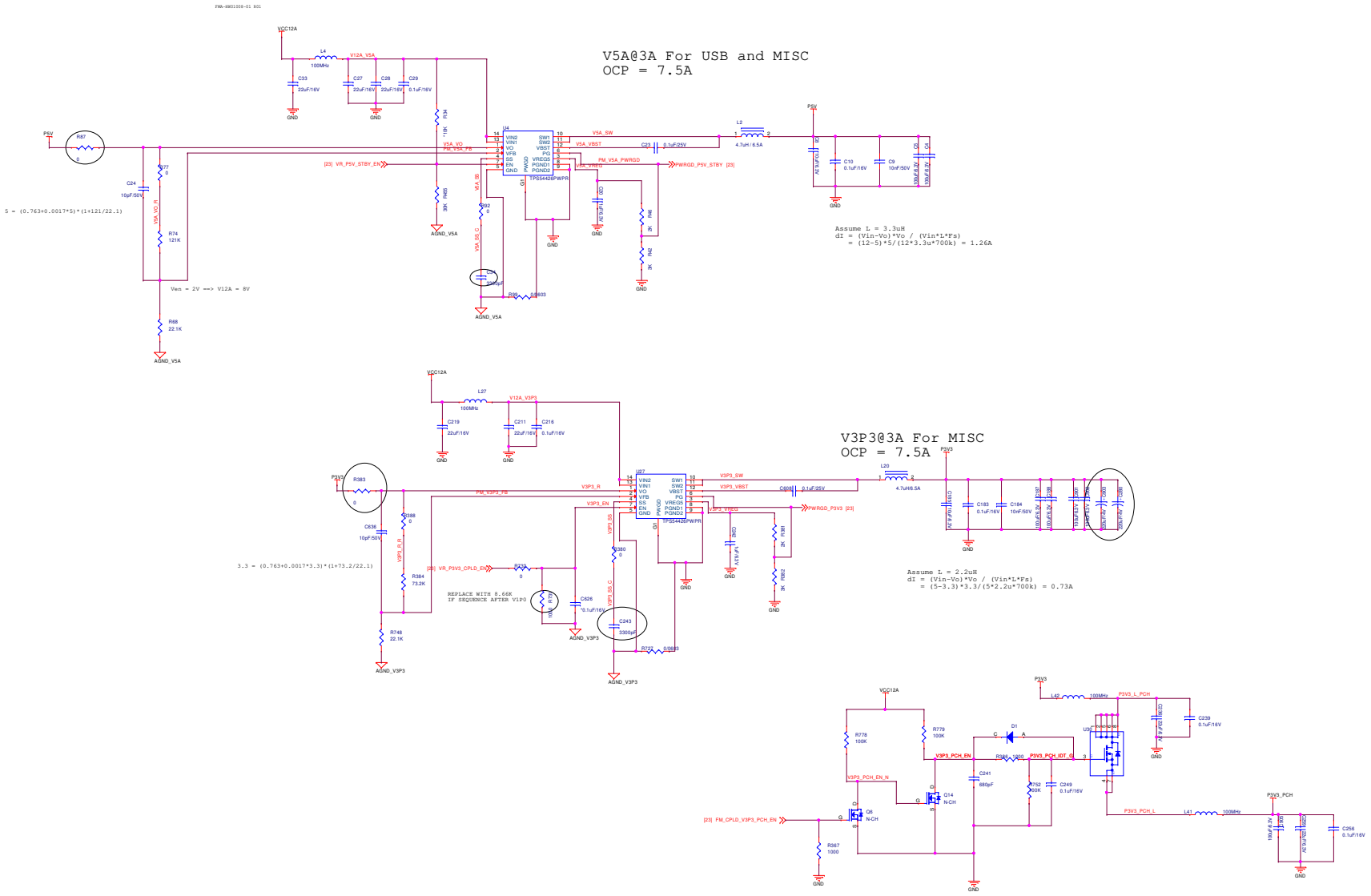

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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| D | 30_P1V2_VDDQ_DDR4_VPP_P06 | VTT Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 30 of 39



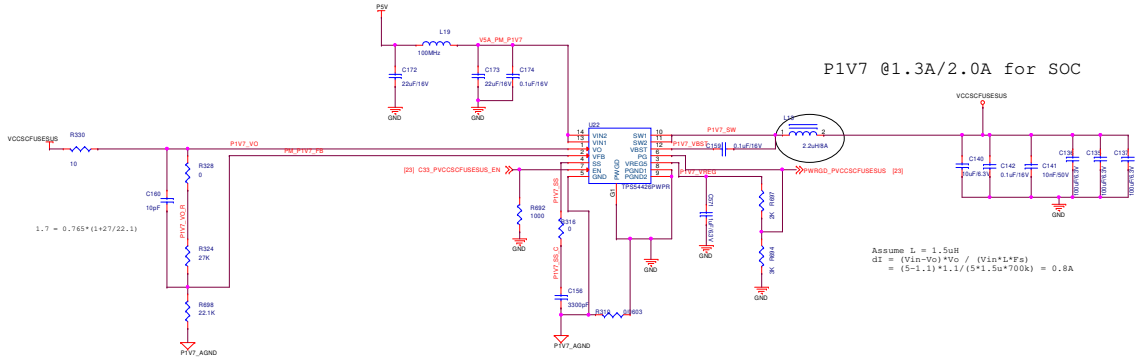

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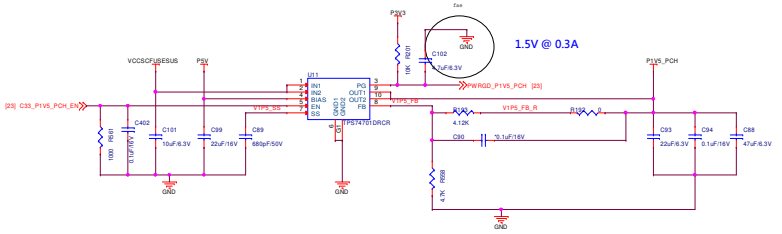
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| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

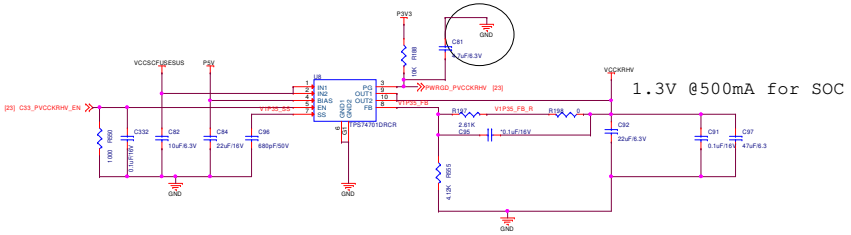
| Size | Page Name | Engineer |
|---|---|---|
| D | 31_P3V3_P5V | Kai Chuang |

Date: Thursday, July 05, 2018 Sheet 31 of 39




1.5 = 0.8*(1+ 4.12/4.75)




1.3 = 0.8*(1+ 2.61/4.12)

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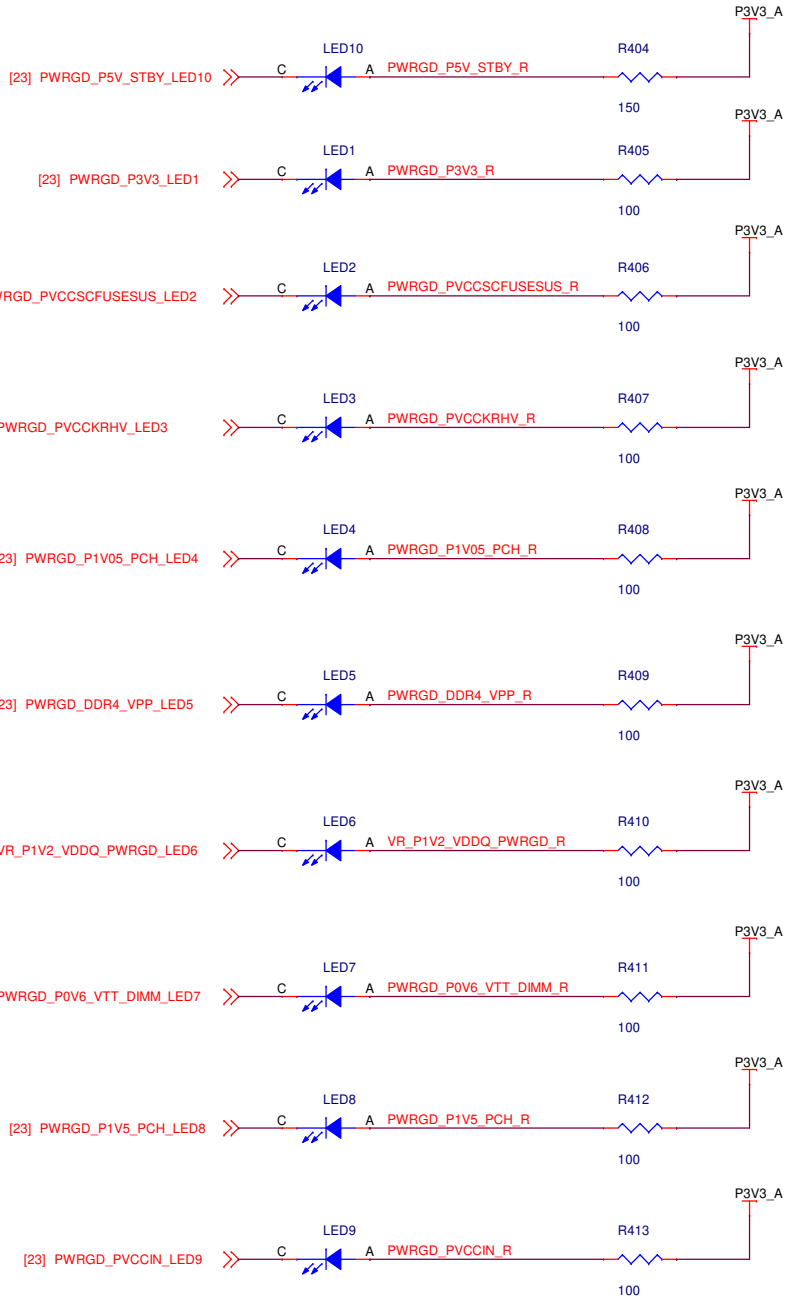
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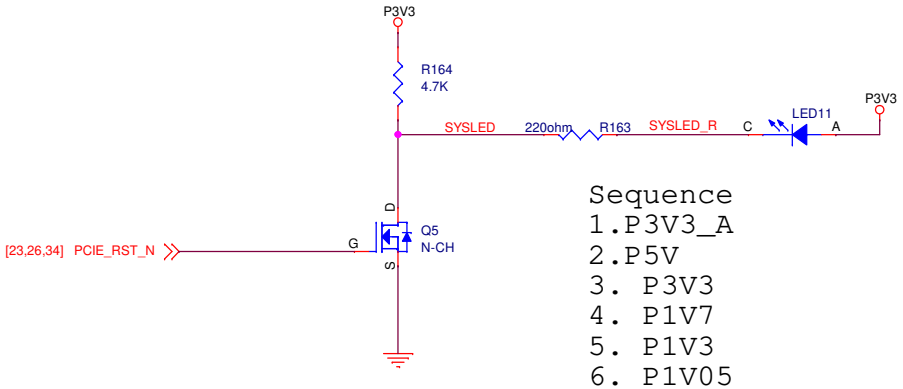
| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

| Size | Page Name | Engineer |
|---|---|---|
| D | 32_1.3V_1.7V_P1V5_PCH | Kai Chuang |

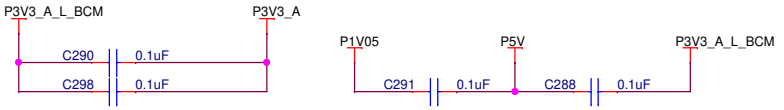
Date: Thursday, July 05, 2018 Sheet 32 of 39

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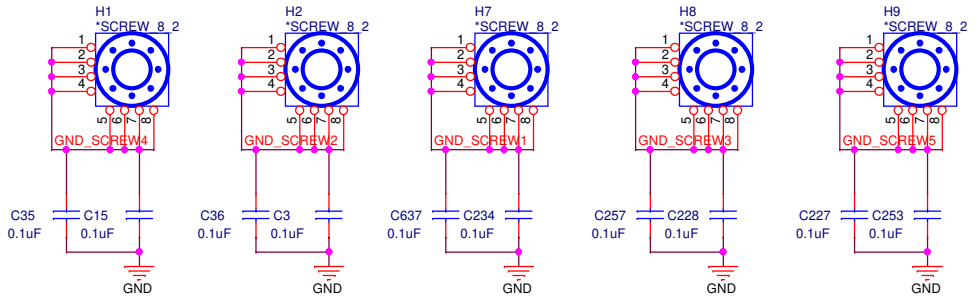



Sequence
1.P3V3_A
2.P5V
3. P3V3
4. P1V7
5. P1V3
6. P1V05
7. VPP
8. VDDQ
9.VTT / VCCIN / P1V5 /




**Screw footprint already use OSP footprint**




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| | | |
|---|---|---|
| Model Name: BDX-DE CPU Board | | Rev: R0A |
| Size: B | Page Name: 33_DEBUG LED | Engineer: Kai Chuang |
| Date: Thursday, July 05, 2018 | Sheet 33 of 39 | |

FMA-HW01008-01 R01

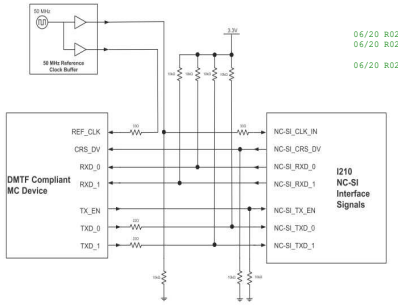



Figure 12-14.NC-SI Connection Requirements - Single-Drop Configuration

| | |
|---|---|
| 00 | MB is Switch System |
| 01 | MB is X86 System |

| S | Function Table |
|---|---|
| L | B0=A BMC |
| H | B1=A (Default) CPU |

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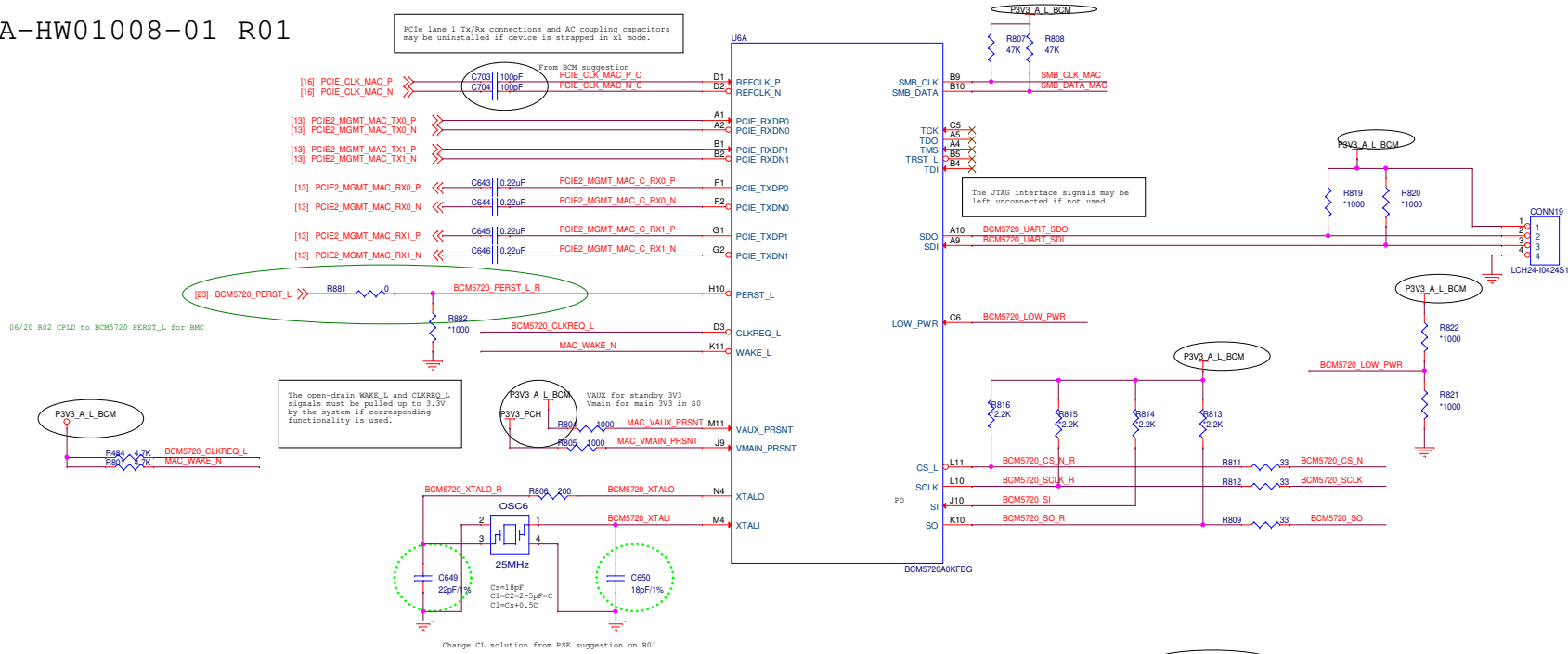
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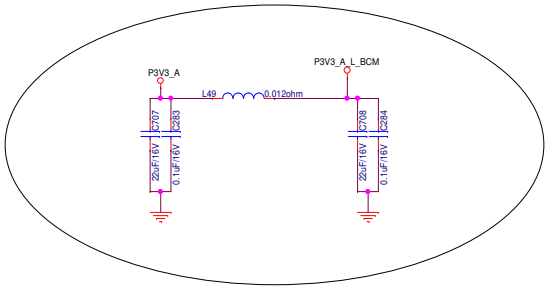
| Model Name | Rev |
|---|---|
| BDX-DE CPU Board | R0A |

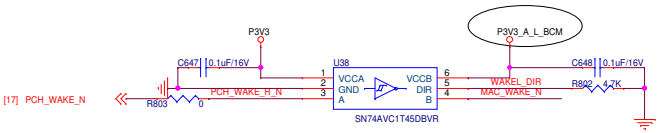
| Size | Page Name | Engineer |
|---|---|---|
| C | 34_BMM CONN | Kai Chuang |

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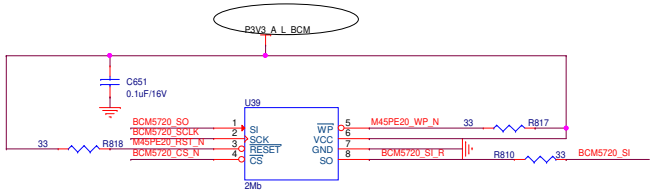




*Table 12: NVRAM Strapping (Cont.)*

| NVRAM Interface Mode or Vendor Part Number | Device Density | Strapping Combination | | | |
|---|---|---|---|---|---|
| | | SO | SI | CS_L | SCLK |
| AT45DB041D (Atmel flash)[a] | 4 Mbit | 0 | 1 | 1 | 0 |
| AT45DB081D (Atmel flash)[a] | 8 Mbit | 0 | 1 | 1 | 1 |
| M25PE10 (Micron® flash)[b] | 1 Mbit | 1 | 0 | 0 | 0 |
| M25PE20 (Micron flash)[b] | 2 Mbit | 1 | 0 | 0 | 1 |
| M25PE40 (Micron flash)[b] | 4 Mbit | 1 | 0 | 1 | 0 |
| M25PE80 (Micron flash)[b] | 8 Mbit | 1 | 0 | 1 | 1 |
| M45PE10 (Micron flash)[b] | 1 Mbit | 1 | 1 | 0 | 0 |
| M45PE20 (Micron flash)[b] | 2 Mbit | 1 | 1 | 0 | 1 |
| M45PE40 (Micron flash)[b] | 4 Mbit | 1 | 1 | 1 | 0 |
| M45PE80 (Micron flash)[b] | 8 Mbit | 1 | 1 | 1 | 1 |

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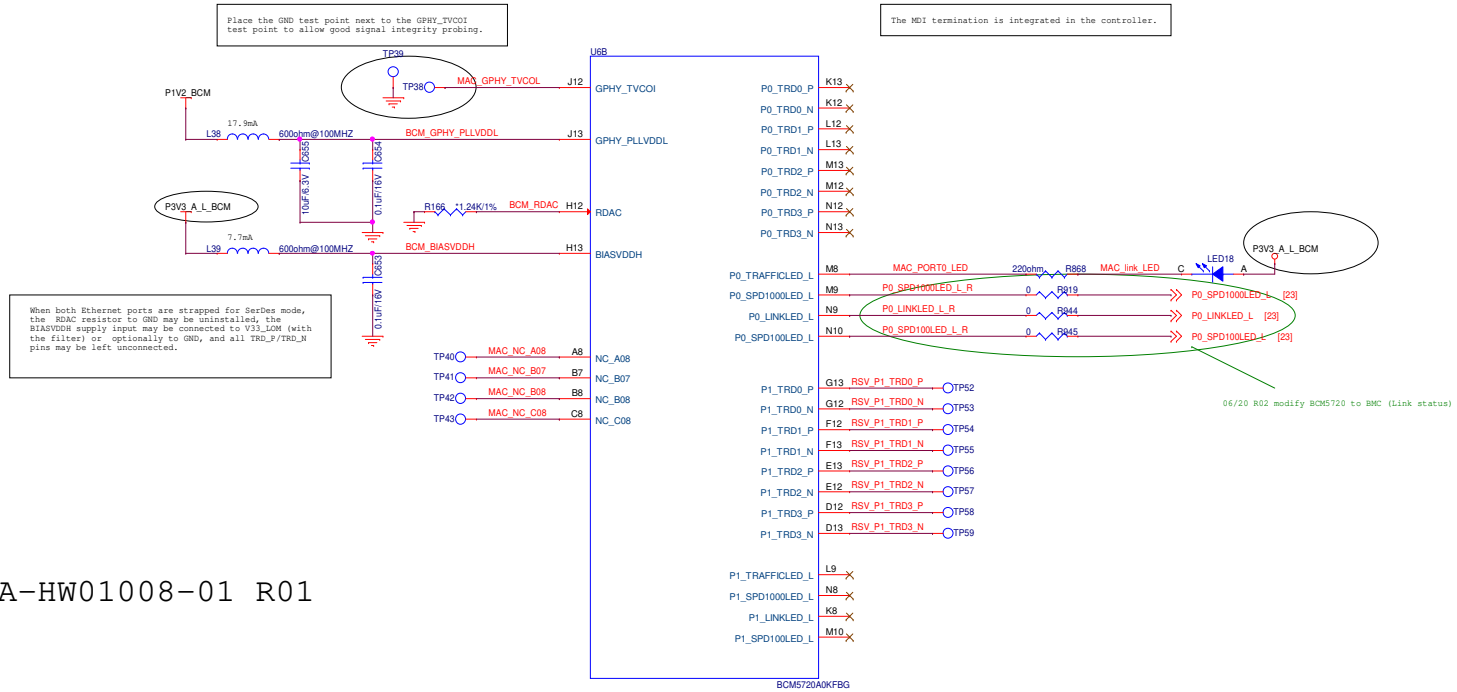
PCI-E, XTAL, NVRAM, DEBUG

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| C | 35_MAC_PCIE_NVRAM_DEBUG | Kai Chuang |

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GPHY PORTS, LEDS

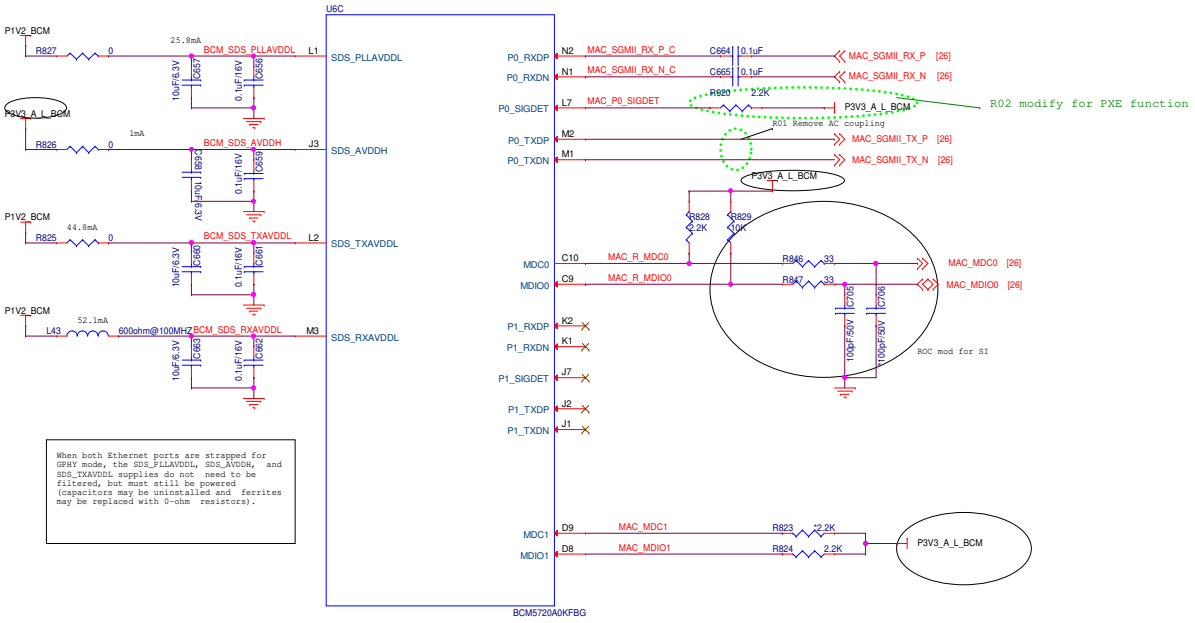
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The MDC[1:0] pins are strapped at POR to select the mode for each Ethernet port according to the table shown. MDC[1:0] are pulled down internally.

When a SerDes mode port is connected to an external SGMII to GPHY bridge, the corresponding MDC/MDIO pins should connect to the management port of the SGMII to GPHY bridge.

| MDC1 | MDC0 | Ethernet Port 1 | Ethernet Port 0 | |
|---|---|---|---|---|
| 0 | 0 | GPHY | GPHY | |
| 0 | 1 | GPHY | SerDes | (by default) |
| 1 | 0 | SerDes | GPHY | |
| 1 | 1 | SerDes | SerDes | |

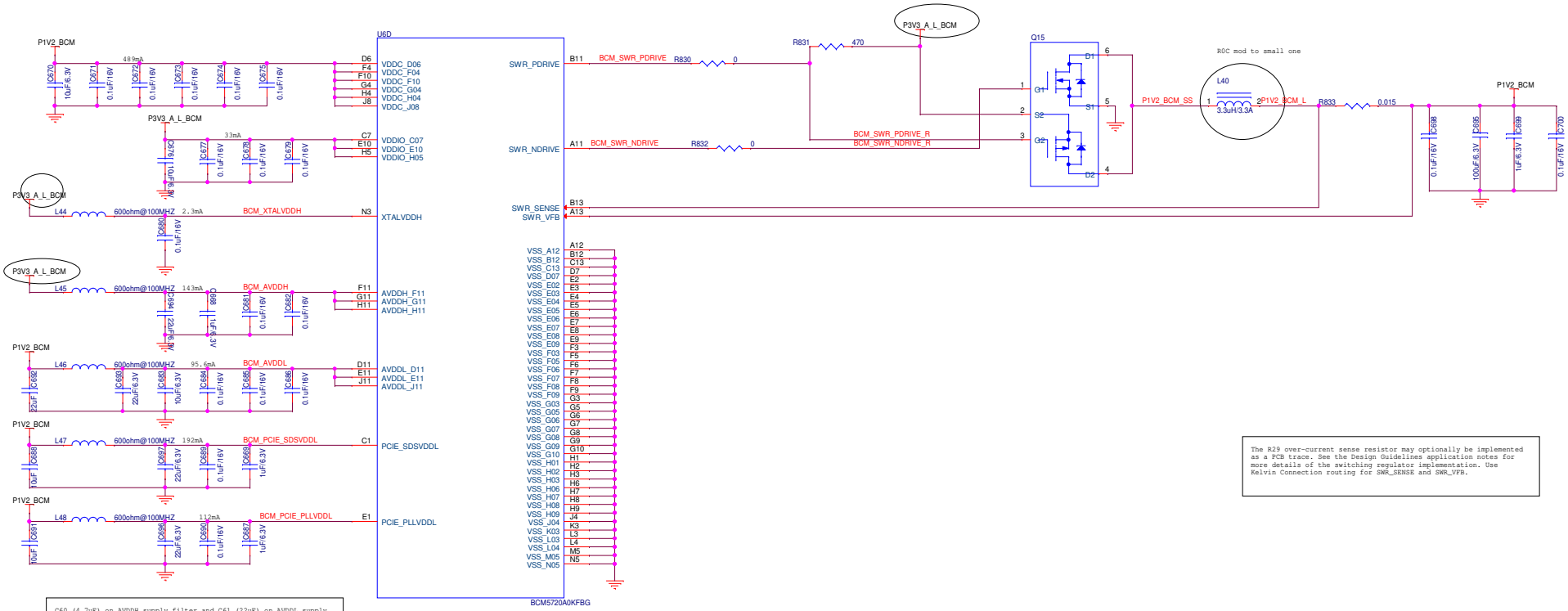
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C60 (4.7uF) on AVDDH supply filter and C61 (22uF) on AVDDL supply filter are the minimum requirement on the EEE-enabled platform. Higher bulk capacitance may be used for smaller voltage transients.

For AVDDL filter, C52 (4.7uF) and C61 (22uF) can be combined into a single 27uF or larger capacitor in designs where EEE will be used. A 4.7uF is the minimum requirement if EEE is not used.

The R29 over-current sense resistor may optionally be implemented as a PCB trace. See the Design Guidelines application notes for more details of the switching regulator implementation. Use Kelvin Connection routing for SWR_SENSE and SWR_VFB.

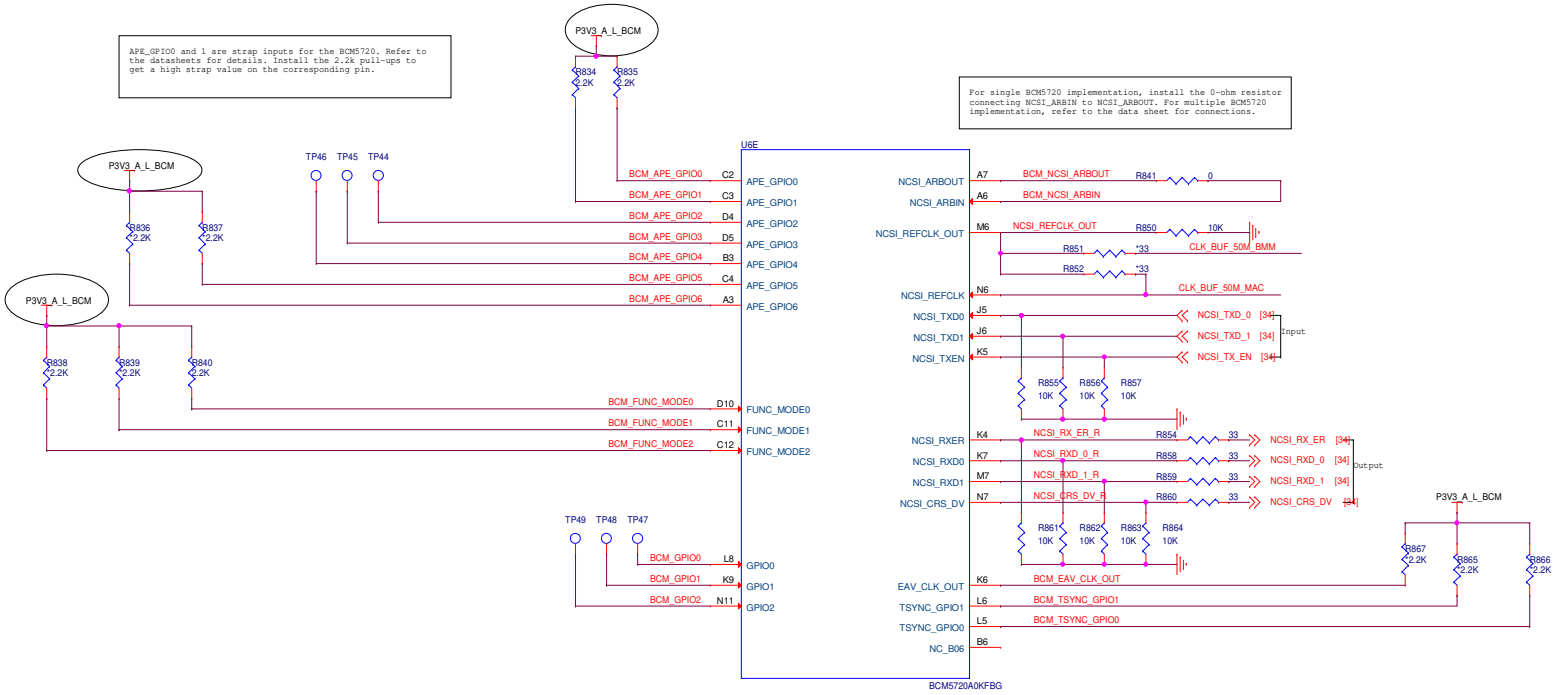
FMA-HW01008-01 R01

POWER

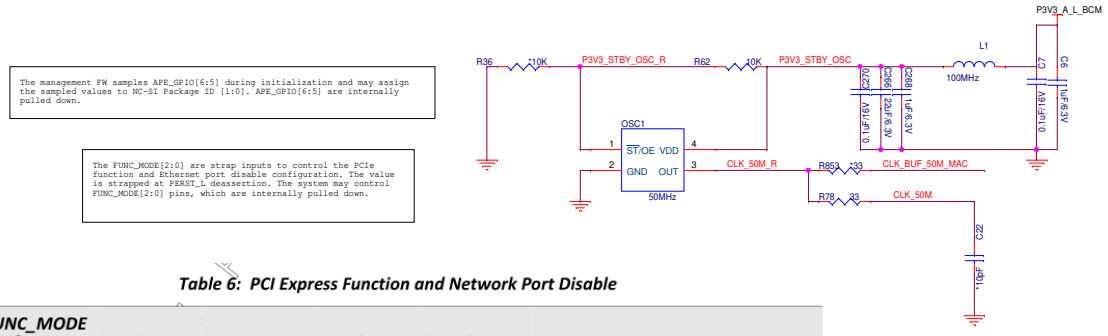
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| Size: C | Page Name: 38_MAC_POWER | Engineer: Kai Chuang |
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**NC-SI, GPIO, MODE STRAPPING, TIME SYNC**



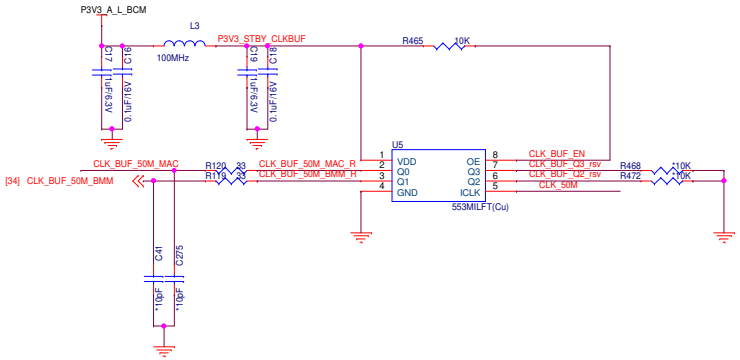




***Table 6: PCI Express Function and Network Port Disable***

| *FUNC_MODE [2:0]* | *Port 0* | *Port 1* | *Function 0* | *Function 1* | *Comments* |
|---|---|---|---|---|---|
| 000 | Enabled | Enabled | Visible | Visible | Default configuration. |
| 001 | Enabled | Disabled | Visible | Invisible | No host traffic through Port 1. |
| 010 | Enabled | Disabled | Visible | Visible | No host traffic through Port 1, but PCIe Function 1 remains visible as a dummy function. |
| 011 | Disabled | Enabled | Visible | Visible | No host traffic through Port 0, but PCIe Function 0 remains visible as a dummy function. |
| 1xx | Disabled | Disabled | Invisible | Invisible | No host traffic through either port. |

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